Czech Technical University in Prague

Faculty of Electrical Engineering
Department of Microelectronics

# Diploma Thesis

Design of a standard cell library in STSCL technology
for AMS 180 nm process

Gordon Neue
Prague 2015

České vysoké učení technické v Praze
Fakulta elektrotechnická

katedra mikroelektroniky

# ZADÁNÍ DIPLOMOVÉ PRÁCE

Student: **Bc. Gordon Neue**

Studijní program: Komunikace, multimédia a elektronika
Obor: Elektronika

Název tématu: **Návrh knihovny standardních buněk v technologii STSCL pro proces AMS 180 nm**

***Pokyny pro vypracování:***

Navrhněte knihovnu standardních buněk STSCL pro využití v ASIC čipech pro sběr dat v nízko-šumových aplikacích. Knihovna musí obsahovat všechna standardní logická hradla, podpůrné obvody pro generování biasovacích napětí a obvody převodníků logických úrovní. Simulací ověřte správnou funkci navržených obvodů a proveďte charakterizaci základních vlastností. Nakreslete layout všech buněk. Zvolte rozložení layoutu tak, aby buňky bylo možné jednoduše vedle sebe složit do mříže, aniž by došlo ke vzniku DRC chyb. Je také žádoucí, aby napájecí a biasovací vodiče automaticky na sebe navazovaly. Navrhněte testovací obvody využívající navržená logická hradla - jednoduchý 8-bitový SAR ADC a 40-ti bitový čítač pro využití v ASIC čipech pro detektory ionizujícího záření. Navrhněte potřebné analogové obvody pro ADC - diskriminátor a zpětnovazebný DAC. Finální design musí být bez DRC a LVS chyb. Použitá technologie je AMS 180 nm, šest vrstev kovů, pouze 1,8 V tranzistory, žádné trojité jámy.

***Seznam odborné literatury:***

[1] Extreme Low-Power Mixed Signal IC Design, Tajalli A., Leblebici Y. Springer 2010, ISBN 978-1-4419-6478-6
[2] CMOS: Circuit Design, Layout, and Simulation, 3rd Edition, Baker R. J., Wiley-IEEE Press 2010, ISBN: 978-0-470-88132-3
[3] The Art of Analog Layout, 2nd Edition, Hastings A., Prentice Hall 2005, ISBN: 978-0131464100

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V Praze dne 18. 11. 2015

Czech Technical University in Prague
Faculty of Electrical Engineering

Department of Microelectronics

# DIPLOMA THESIS ASSIGNMENT

Student: **Bc. N E U E Gordon**

Study programme: Communications, Multimedia, Electronics
Specialisation: Electronics

Title of Diploma Thesis: **Design of a standard cell library in STSCL technology for AMS 180nm process**

***Guidelines:***

Design a STSCL library of standard cells to be used in low noise data acquisition ASICs. The library must contain all the basic logic cells used in digital circuits, the necessary support circuits to generate the proper bias voltages and the circuits necessary to interface STSCL logic levels to and from standard CMOS logic circuits. Through simulation perform the characterization of the logic cells. Draw the layout of all cells. Chose a layout so that the cells are easily buttable into a grid in such a way that bias voltage rails and power rails are automatically connected by placing cells next to each other. Ensure that placing cells randomly next to each other does not create DRC errors. Design a few test IP cells - a simple 8 bit SAR ADC and a 40bit timer counter to be used in nuclear detector ASICs. Design the necessary analog circuitry for the ADC - a zero offset discriminator and the feedback DAC. The final design must be DRC and LVS clean. The technology node is AMS 180nm, six metal layers, only 1.8V transistors, no triple wells.

***Bibliography/Sources:***

[1] Extreme Low-Power Mixed Signal IC Design, Tajalli A., Leblebici Y. Springer 2010, ISBN 978-1-4419-6478-6
[2] CMOS: Circuit Design, Layout, and Simulation, 3rd Edition, Baker R. J., Wiley-IEEE Press 2010, ISBN: 978-0-470-88132-3
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Diploma Thesis Supervisor: **Ing. Ondřej Šubrt, Ph.D.**

Valid until 28. 2. 2017

L.S.

prof. Ing. Miroslav Husák, CSc.
Head of Department

prof. Ing. Pavel Ripka, CSc.
Dean

Prague, September 30, 2015

**Abstrakt:** Práce se zabývá návrhem knihovny standardních buněk STSCL pro využití v ASIC čipech v detektorech ionizujícího záření. Knihovna byla navržená v technologii AMS 180 nm. Knihovna obsahuje všechna standardní logická hradla potřebná pro syntézu digitálních obvodů. Po krátkém úvodu do problematiky logiky pracující v proudovém režimu, nasleduje přehled návrhu a vlastností logických hradel realizovaných v technologii STSCL. Závěrem práce je popsán návrh dvou obvodů využívajících STSCL hradla - 40-bitový TOA čítač a 8-bitový SAR ADC.

**Abstract:** This thesis deals with the design of a STSCL logic library to be used in nuclear detectors. The design was realized in the AMS 180 nm process. The library contains all basic logic gates necessary for the synthesis of digital circuits. A brief introduction into topic of constant current mode logic is provided, followed by an overview of the design process and properties of STSCL gates. Finally the design of two IP cell utilizing STSCL gates is provided - 40 bit TOA counter and a 8 bit SAR ADC.

**Čestné prohlášení**

Prohlašuji, že jsem zadanou diplomovou práci vypracoval sám s přispěním vedoucího práce a používal jsem pouze literaturu v práci uvedenou. Dále prohlašuji, že nemám námitek proti půjčování nebo zveřejňování mé diplomové práce nebo její části se souhlasem katedry.

V Praze dne 10. 1. 2015 Gordon Neue

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# 1 Introduction

STSCL stands for Sub-Threshold Source Coupled Logic. It is a class of logic cells operating in the current mode regime. A constant current is flowing through the logic gates at all times, independently of logic activity. This class of logic cells is similar to the better known SCL (Source Coupled Logic) for CMOS processes and the earlier ECL (Emitter Coupled Logic) for bipolar processes. Constant current logic was invented by Hannon S. Yourke in the year 1956, at that time still realized with discrete bipolar circuit components[1]. SCL followed after the invention of the CMOS process. The current steering logic families ECL and SCL have a long tradition, being used for the highest speed logic circuits on their particular process nodes. STSCL is similar to SCL. STSCL is a logic class invented in 2008 by Armin Tajalli and Yusuf Leblebici[2]. STSCL addresses one of the major drawbacks of SCL and ECL logic - power consumption. STSCL shares many of the design principles, circuit elements and features with these preceding current mode logic technologies. It too uses differential signaling to represent logic levels, meaning that a logic variable is expressed by the relative voltages on two signal wires instead of the voltage on a single wire against ground.

To exemplify the difference between the standard CMOS logic family and the current mode logic family, let us have a look at the most basic logic gate - the inverter. Figure 1 displays the simplified schematic representation of a differential, constant current logic inverter gate versus a standard CMOS inverter gate. The CMOS inverter gate (A) consists of two stacked transistors. When the logic input level is not toggling, the CMOS gate displays almost no power consumption (only leakage currents in the order of fA contribute to the static power consumption). In the CMOS inverter gate (A) only one of the stacked transistors is opened at a given static input logic level, the second transistor is always closed. Note that both transistors might be open only for a short period of time, when the input logic signal transitions from one logic level to another logic level. The current mode inverter gate (B), like SCL and STSCL, has a constant static current flowing through it independently of the activity of the logic signals. This current flowing constantly through the gate is being called the tail current, $I_{tail}$.

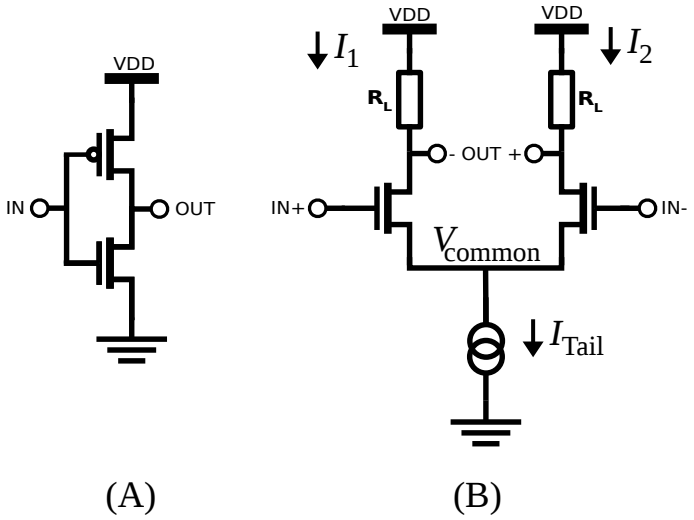


Figure 1: Simplified schematic of a CMOS inverter (A) and a SCL inverter (B).

The current mode logic inverter, (B) on figure 1, has a constant current source attached to the sources of the differential pair (the transistors , whose gates are connected to the input pins IN+ and IN-). The current source $I_{tail}$ causes the source voltage $V_{common}$ of the differential pair to drop to such a value, that the sum of the currents $I_1$ and $I_2$ are equal to the tail current $I_{Tail}$. This happens because $V_{common}$ represents the source voltage of the transistors in the differential pair and by changing $V_{common}$ the effective gate-source voltage is being modulated. By applying a differential input voltage to the input terminals of the gate (B) the tail current $I_{tail}$ can be alocated to flow either through the left or the right load resistor $R_L$, generating thus a differential output voltage on the OUT+ and OUT- terminals. The exact ratio in which the tail current is being divided between the load resistors in response to the differential input voltage is dependent upon the regime in which the transistors are being operated (saturation or sub threshold), see section 5.2.

The main difference between the SCL and the STSCL logic families is hidden in how the load resistors $R_L$ form figure 1 are being implemented. Figure 2 displays the various ways of how the load resistors can be implemented. The schematic structure of the various STSCL gates can be found in section 6.

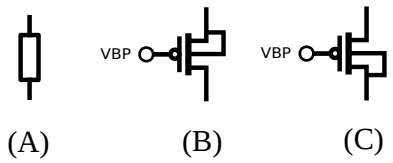


Figure 2: The various ways how load devices can be implemented: (A) By resistor, this is how it is done in SCL logic, (B) active PMOS load device with the well tied to $V_{Supply}$ and (C) active PMOS load device with the well tied together with the drain, this is how STSCL load devices are implemented.

From figure 1 it is apparent that the differential logic gate has a more complicated structure than the CMOS gate, the question thus arises why use current mode logic gates at all? There are multiple reasons, why under certain conditions using the more complex current mode logic is reasonable:

- CMOS logic is very noisy. The current spikes on the supply lines typical for digital CMOS circuits is a major noise contributor in mixed signal circuits. Current mode logic does not have that drawback.
- The differential nature of the logic signals makes it possible to improve the noise margin in low supply voltage environments, since the possible voltage swing can be theoretically up to twice the supply voltage.
- The differential nature of the logic signals reduces the susceptibility to common mode noise sources.
- In CMOS circuits the logic voltage swing must be rail-to-tail. If the noise environment allows the reduction of the logic signal voltage swing, the speed of the gates can be significantly increased. SCL gates can be operated at significantly higher clock speeds than CMOS.
- SCL and STSCL logic gates offer the option to dynamically control the gate speed via the tail current. In STSCL gates it is additionally possible to control the voltage swing itself. These degrees of freedom make it possible to dynamically adjust the speed and power consumption of digital circuits. With STSCL a designer can chose the optimum gate speed, noise margin and power consumption.
- Removing the current spikes on the supply line makes it easier do design the power distribution network on the ASIC. In CMOS logic the power

distribution network must be designed for the peak current; in current mode logic the power distribution network can be designed for the mean current.

- Removing the current spikes on the supply line rails also reduces the risk of electro migration.
- STSCL logic can be operated with well defined behavior in sub threshold regime, allowing for the design of logic circuits at very low voltages.
- STSCL gates can be biased with extremely low tail currents in the order of pA making them, in combination of very low supply voltages, perfect for ultra low power applications.

There is an empirical rule to the design of a logic library (This rule applies to any circuit design be it digital or analog). There are three main design criteria (noise margin, speed, power consumption) which must be met when designing a logic library. An ASIC designer is free to set the benchmark of two of those criteria according to his desire, but the third criterion is then being imposed upon him as a consequence of his prior choice. For example if one choses to have a high noise margin and speed, then one must accept a high power consumption. Chosing low power and high speed will lead to a miserable noise margin. In the design process are thus three criteria to be met, but just two effective degrees of freedom to achieve so. Not any combination is possible and even from those combinations that would be allowed by the laws of nature, not any is achievable for a given logic family. For example, it is very difficult to operate CMOS type logic in the sub threshold regime, with the supply voltage bellow the threshold voltage. The reason being, that due to PVT variations the input voltage level, at which the gate toggles, can move in a wider range in sub threshold regime and as we reduce the supply voltage, the noise margin drops even faster. Figure 3 gives a rather conceptual overview of which logic family is best for which type of application (the actual achievable regions will strongly depend upon which process is being considered).

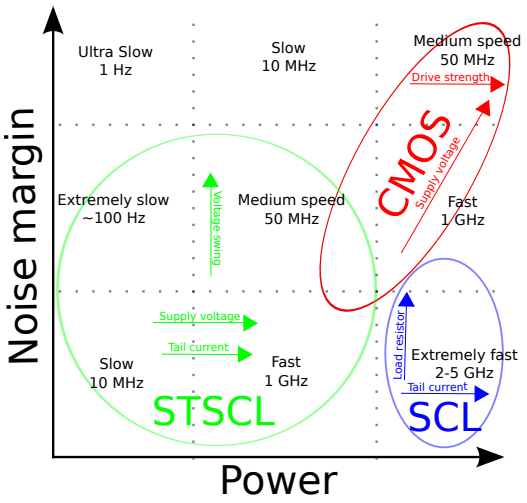


Figure 3: A conceptual diagram of which speed/power/noise margin regions are being covered by which logic family and how the various degrees of freedom affect the behavior of the gates. Power for CMOS is as assumed at maximum toggling speed.

As can be seen CMOS is best for very noisy environments, but not for very low power. SCL is best best for high speed circuits, but with very high power consumption. STSCL is superb in low noise, extreme low power applications, but does so by being very slow.

# 2 CMOS switching noise

The main reason, why it was decided to experiment with STSCL in the scope of this thesis, is their high potential in low noise mixed signal applications for nuclear detectors. To better understand the effect of switching noise let us compare the supply current drawn by a CMOS inverter gate and STSCL inverter gate, see figure 4.

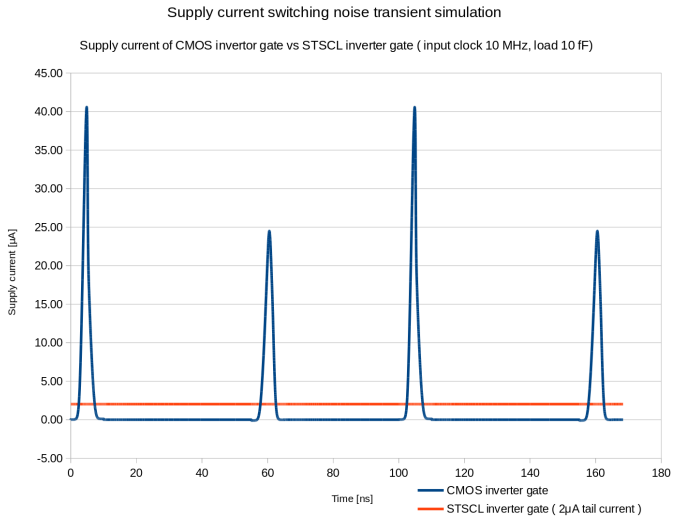


Figure 4: The current spikes of a 1x CMOS inverter versus the supply current of a STSCL inverter (both have the same input clock).

A major advantage of current mode logic families lies in the fact that the power distribution network can be dimensioned for the mean current instead of the peak current. The peak current of digital circuits can reach very high values compared to the average current implied by the mean power consumption. The power distribution network is a major source of headache for digital designers. In CMOS circuits it is critical to keep the resistance of the power distribution network as low as possible. To better illustrate the effect that the resistance of the power distribution network has upon the operation of digital circuits, let us consider the fact that the lowest drive strength inverter in the AMS 180 nm standard cell library, produces a current spike of 40 $\mu$A ($V_{dd}$= 1.8 V, $\tau_{rise/fall}$ = 1 ns, $C_{load}$ = 10 $fF$), see figure 4. The minimum supply voltage $V_{dd}$ is 800 mV ($V_{dd}$ must be reliably above the highest threshold voltage of the transistors used). For a supply voltage of 1.8 V our head room is thus only 1 V. If we now assume a resistance of 1 $\Omega$ for each branch of the supply rails, we obtain that if we tried to toggle more than 12500 inverters simultaneously the voltage on the $V_{dd}$ rail inside of the chip would drop to 1.3 V and the ground rail bounces to 500 mV. From the these consideration thus follows that in a purely digital circuit no more than 10K simultaneous switching gates may be connected to each Siemens of supply rail. In mixed signal circuits the impact of the simultaneous switching

noise becomes even more severe. In mixed signal circuits there exists the additional risk of injecting the noise from the digital circuits into analog circuits. There are multiple pathways by which noise from digital circuits can enter the analog domain on the chip level and the PCB level. The main pathway is through substrate coupling. The current spikes of the toggling logic do not only cause voltage spikes on the supply rails, but also in the chip substrate. Additional pathways for noise injection are at the circuit board level, where the currents spikes inductively couple with analog signal bearing traces and, in very low noise applications like nuclear detectors, even the cross talk between chip wire bonds is a major issue.

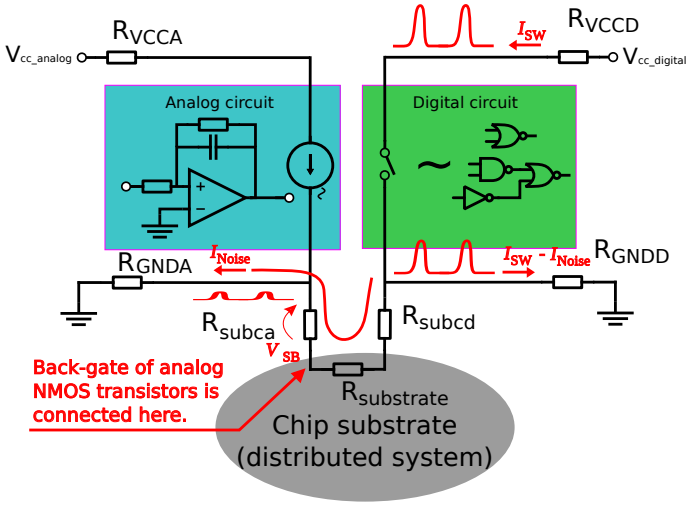


Figure 5: A simplified model to understand how substrate injection occurs in mixed signal CMOS circuits without the triple well process option.

Substrate coupling occurs when the current spikes of digital CMOS circuits create voltage spikes on the ground wires due to the non zero resistance of those ground wires. P substrate CMOS technology requires the bulk of NMOS transistors to be locally tied to the ground node. To suppress back-gate effects and to prevent latch-ups CMOS circuits have a ground to substrate contact close to each NMOS transistor. These local substrate contacts have in the AMS 180 nm process an internal resistance in the order of hundreds to a few kΩs (the actual size depends upon the transistor size and how much area the designer wishes to sacrifice for substrate contacts). The resistance of these substrate contacts on figure 5 is designated with $R_{subca}$ and

$R_{subcd}$. As can be seen on figure 5 moving the voltage on the digital ground node as will thus also locally lift the substrate voltage. Since the analog circuits and the digital circuits do share the substrate (in case of a process without the triple well option), the analog circuits, which have a separate ground net, will see the substrate moving relative to this analog ground. It is difficult to calculate the exact value of $R_{substrate}$ since the substrate must be modeled as a distributed system. As ASIC designers we are often not interested in the exact solution, but rather in the worst case scenario estimate. Calculating the exact value of $R_{substrate}$ is thus not necessary. The real world substrate resistivity is roughly 10 $\Omega \cdot cm$, but in the worst case scenario, we can assume the substrate to act as a perfect conductor and that it has no other ground connections other than the two being displayed. We thus for analytical reasons assume $R_{substrate} = 0\ \Omega$. We can now calculate the switching noise that an analog NMOS transistor receives on its back-gate. The peak voltage will be:

$$V_{BS,max} = I_{Switching,max} \frac{R_{GNDD} \cdot R_{subca}}{R_{GNDD} + R_{subcd} + R_{substrate} + R_{subca} + R_{GNDA}} \quad (1)$$

Since we are interested in the worst case scenario and since resistance in this case is always a positive quantity, we can make the following estimate for the worst case noise voltage:

$$V_{BS,max} < I_{Switching,max} \cdot R_{GNDD} \quad (2)$$

Analog circuits often use NMOS transistors to set the bias currents in these circuits. The bias NMOS transistors are susceptible to being modulated through the back-gate, if the substrate voltage is pulsating beneath them.

The above stated considerations show why in mixed signal circuits for each Siemens of supply rail conductivity only hundreds of inverters may be connected before noise substrate coupling becomes and issue. Substrate coupling is a distributed phenomena and very difficult, if not impossible to simulate. It is also to be noted, that such noise will not be added white Gaussian noise (AWGN) since it is to be expected that in mixed signal circuits the operation of the digital circuits will somehow be correlated with the operation of the analog circuit and thus not statistically independent and substrate coupling

can therefore be very difficult to debug. The uncertainty surrounding the risk of substrate coupling and the difficulty of simulating said phenomena show why current mode logic is very attractive for low noise mixed signal applications. Instead of reducing the $R_{GNDD}$ parameter in equation 2 we attack the second parameter, $I_{Switching,max}$. Whereas we can never realistically achieve a zero ground wire resistance, achieving nearly zero switching current is possible.

There are many mitigation strategies, to reduce the risk of noise injection, proper grounding techniques and using a triple well process being the most common ones, but these options never remove the primary noise source. Using constant current logic is a very efficient technique to get rid of the injected noise, since it addresses the fundamental cause for the noise - the current/voltage spikes on the power rails. Figure 4 displays the current spikes observed on a CMOS inverter and a STSCL inverter in AMS 180 nm technology. As can be seen the STSCL gate produces no visible current spike while switching, this comes at the price, that this current has to be flowing at all times while the IP cell is in operation.

# 3 Power consumption

The average power consumption of a CMOS inverter gate is given by equation 3 and the power consumption of an STSCL inverter gate is given by equation 4. Whereas STSCL has for a given tail current a constant power consumption independently of logic activity, CMOS gates do display a power consumption strongly dependent upon toggling speed. Figure 6 displays the simulated power consumption of an AMS 180 nm standard cell CMOS inverter versus the toggling clock speed. The bulk of the power consumption of CMOS digital circuits is given by its dynamic switching currents.

$$P_{CMOS\,Inverter} = V_{supply} \cdot I_{leakage} + C_{pd} \cdot f_{toggling} \cdot V_{supply}^2 \tag{3}$$

$$P_{SCL\,Inverter} = V_{supply} \cdot I_{tail} \tag{4}$$

The capacitance $C_{pd}$ in equation 3 is being called the power dissipation capacitance. It is not simply just the output capacitance of the gate; it incorporates a plethora of other effects. For example when the logic signal transitions from one level to the other, there will be a short moment when

both the PMOS and a NMOS devices in the CMOS gate are opened briefly. This transitional current, that passes straight trough both open transistors, is in this simple model also covered by assigning a value to the $C_{pd}$ capacitance larger than the actual output capacitance. The effective value of the power dissipation capacitance therefore depends upon the rise/fall times of the logic signals. It is also not entirely clear what is being meant by logic signal transitions, since there may not be a unique way to drive a logic gate (with the notable exception of the inverter gate). The model of equation 3 is thus just an approximation.

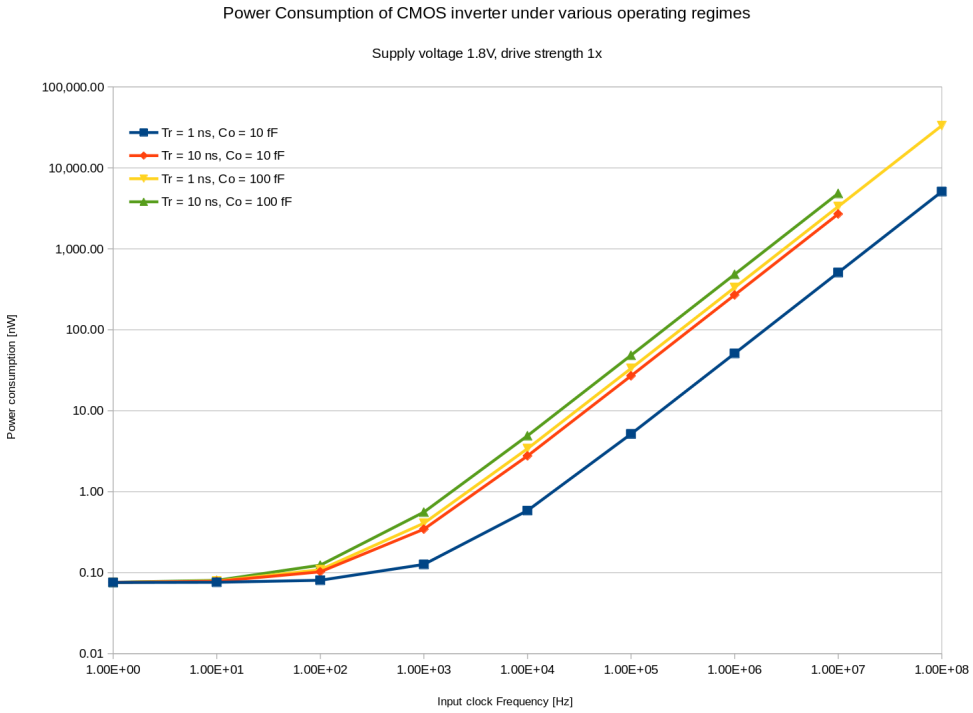


Figure 6: Simulation of CMOS inverter power consumption under various operating conditions.

Figure 6 displays the simulated power consumption of a single CMOS inverter gate. As can be seen the power consumption for the frequency of 1 MHz is for the case of 1 ns rise/fall times and load capacitance of 10 fF equal to 51 nW. If we would like to replace this gate with a SCL type of gate, which consumes a constant current and thus has a constant power consumption and

would like to achieve a similar power consumption, we would need to operate the SCL gate with a tail current of $I_{tail} = 28.3\,nA$ ($V_{supply} = 1.8\,V$). If we would operate the SCL gate with such a small current, the load resistors $R_L$ in the SCL gate from figure 1 would have to be in the magnitude of 10s of MΩs. The load resistors $R_L$ determine the voltage swing on the output of the gate. If they are to small for a given tail current, then the output voltage swing of the gate might not be sufficiently high to distinguish reliably the logic level the in the presence of noise. Transients one the power rails could in this case easily toggle flip-flops and cause logic hazards. One of the major limitations of contemporary CMOS processes is the difficulty of creating large resistors. The resistivity of materials available to the designer for resistors is not high enough and creating large passive resistors on the ASIC is very area intensive. It is technologically problematic to deposit high resistivity polysilicon. With only small resistors available, it meant in the past that SCL gates needed to be operated with relatively large tail currents in order to achieve the desired voltage swing. This meant that SCL gates are only power efficient in very high frequency/high activity digital circuits. At toggling speeds above 1 GHz SCL gates become competitive with CMOS gates in terms of power consumption. The region above 1 GHz clock frequency is also the traditional area in which such gates have found their applications. A typical application for SCL gates are the the feedback network dividers in PLLs which must run at the VCO clock speed, the digital circuits in the front end of software defined radio ASICs which must run on the RF frequency of the carrier signal, ultra high speed ADCs and similar circuits.

If we want do use SCL type gates efficiently at lower toggling speeds we need to find a way how to implement the load resistors without having to use polysilicon resistors. This was successfully achieved by A. Tajalli, E. Vittoz, E. Brauer and Y. Leblebici who published in 2007 their groundbreaking paper "Ultra low power sub threshold MOS current mode logic circuits using a novel load device concept" [2]. With the new load device structure and biasing mechanism it became possible to create well behaved MOS resistors in MΩ and GΩ range and it became possible to operate SCL gates in the sub threshold regime, therefore STSCL. With high ohmic load devices it is possible to bias the gates with nA and even pA currents, allowing for the design of constant logic circuits that can compete in terms of power consumption with CMOS circuits at much lower toggling speeds. The load devices are created with PMOS transistors, which have their n-well shorted with the drain instead of with the source as usually the case with PMOS

transistors. More on the subject of the load devices in the chapter 5.1.

# 4 Use of STSCL in nuclear detector ASIC design

This work considers the use of STSCL for nuclear detector ASIC design. STSCL offers some very interesting properties in nuclear detector design. A valuable feature of this class of logic is that the tail current is being adjusted via feedback loops which automatically compensate for leakage currents caused by total ionizing dose (TID) damage. Another property in environments of high ionizing radiation, that might prove useful, but yet has to be verified, is the differential nature of STSCL. Particles, especially alpha particles, create upon impact a lot of local free charge in the silicon bulk material. This charge can drift into the active region of MOS transistors and create short transient noise spikes on the logic gates. These transients interfere with the operation of finite state machines and can cause logic hazards and unpredictable behavior. The differential nature of the logic cells and the tight coupling of the differential pairs offers the possibility to have a higher immunity against single event upsets (SEUs). The two features of TID and SEU immunity are interesting, but they are not the main motivation, why STSCL is being investigated for nuclear detector ASICs in this work. The most desirable feature of STSCL for nuclear detector design stems from the fact, that it has a constant supply current, but still can be designed in such away as to have reasonably low power consumption. The charges that are being created by ionizing particles inside of the depleted region of semiconductor detectors are of the magnitude of thousands of electrons. It is the designated goal of the read-out ASIC to measure these minuscule charges created in the depleted region of silicon diode sensor. The desired precision of measurement of this charge packets is of the order of hundreds of electrons. X-ray and gamma photons of the energy range from 10 KeV up to 1 MeV have a long radiation length. In order to detect such photons with good efficiency the volume of the detecting element must be large, which implies that these detectors will simply due to their large geometric structure have a large parasitic self capacitance. A typical parasitic capacitance of a sensor element is in the order of 5 pF for silicon strip sensor and 1 pF for a silicon pixel sensor. The nuclear detector readout ASIC must thus extract

a minuscule charge from a relatively large capacitance. This is usually done with an transimpedance amplifier or a charge sensitive amplifier. In order to achieve a good charge collection efficiency the amplifier, which is sensing the signal in the sensor, must have an extremely low input impedance, which, if one analyzes how a TIA or CSA circuit operates, implies that the amplifier must have a very high forward open loop gain. High gain does not come for free in electronic design. High gain implies either high power consumption or very noisy operation both of which are undesired. The design of the analog front-end circuits for nuclear readout ASIC is a highly complex topic and outside of the scope of this work; it suffices to state that the analog front-end circuits in nuclear readout ASIC require an extreme low noise environment for proper operation.

Table 1 gives an overview of the parameters of the CMOS, SCL and STSCL logic families.

| **Parameter** | **CMOS** | **SCL** | **STSCL** |
|---|---|---|---|
| Current mode | No | Yes | Yes |
| Differential signaling | No | Yes | Yes |
| Minimum $V_{DD}$ | Max($V_{thn}$,$V_{thp}$) | $V_{th}$+$V_{DS,sat}$+$V_{swing}$ | $V_{DS,sat}$+$V_{swing}$ |
| Tail current per gate | N/A | $10\mu A$ up to $1mA$ | $10pA$ up to $10\mu A$ |
| Maximum clock speed | Medium | Very high | Low/Medium |
| Optimum power efficiency | Static circuits | Maximum speed | Low/medium speed |
| Load devices | N/A | Resistors | Active PMOS |
| Static power | Only leakage | Very high | Low/Medium |
| Dynamic power | Scales with frequency | None | None |
| Degrees of freedom[a] | 1 ($V_{dd}$) | 2 ($V_{dd}, I_{tail}$) | 3 ($V_{dd}, I_{tail}, V_{SW}$) |
| VDD, GND noise injection | High | Low | Very low |
| Substrate coupling | High | Low | Very low |
| SEU[b] susceptibility | High[c] | Very Low | Low |
| TID[d] damage | Very high | Very Low | Medium[e] |
| Floating inputs | Dangerous | Medium risk | Medium risk |
| Power gating | Complex | Easy[f] | Easy[f] |
| Peak to mean current ratio | Very high | 1 | 1 |
| Year of introduction | 1963 | 1956 | 2007 |
| Circuit routing complexity | Low | High | Very high |
| Design flow with EDA tools[f] | Digital/Analog | Only Analog | Only Analog |

Table 1: A comparison of the properties of the CMOS versus the current mode logic families. Notes:(a) The number of degrees of freedom designates the number of bias rails that are available after fabrication to adjust the circuit working points/behavior. (b) A Single Event Upset (SEU) is a soft error (change of state) in a digital circuit caused by one single ionizing particle (ion, electron, high energy photon). (c) CMOS SEU susceptibility is significantly reduced if implemented on SOI. (d) TID stands for Total Ionizing Dose. TID can cause a multitude of effects in silicon semiconductors - shifts of threshold voltages, parasitic transistors along trench isolation oxides, increased leakage currents, etc. (e) Expected, but not yet confirmed experimentally. (f) The tail current source inherently present in current mode gates can also be used as a footer sleep transistor if the current source is implemented with a high $V_{th}$ transistor.(f) As of Q3 2015.

# 5 STSCL design consideration

## 5.1 STSCL load device design

Figure 7 displays the IV curve of a PMOS device with the well connected to the source (situation (B) on figure 2). Since the current is the independent variable it is displayed on the x-axis and figure 7 shows the transistor I-V curve in transpose of how it is being displayed usually. The technology is a deep sub-micron process the square law relation apply only approximately, nonetheless in the saturation the they can be expressed as:

$$I_D = \frac{KP_p}{2} \cdot \frac{W}{L}(V_{SG} - V_{THP})^2\big[1 + \lambda(V_{SD} - V_{SD,sat})\big] \tag{5}$$

where

- $I_D$ is the drain current,
- $KP_p$ is the process constant,
- $W$ is the transistor width,
- $L$ is the transistor length,
- $V_{SG}$ is the source to gate voltage,
- $V_{THP}$ is the PMOS threshold voltage,
- $\lambda$ is the channel length modulation factor,
- $V_{SD}$ is the source to drain voltage,
- $V_{SD,sat}$ is the source to drain saturation voltage.

Let us now analyze this equation at the boundary of triode operation and saturation; that is to say we set $V_{SD} = V_{SD,sat}$ we obtain:

$$I_{D,sat} = \frac{KP_p}{2} \cdot \frac{W}{L} \cdot V_{SD,sat}^2 \tag{6}$$

rearranging

$$V_{SD} = \sqrt{\frac{2}{KP_p} \cdot \frac{L}{W} \cdot I_{D,sat}} \tag{7}$$

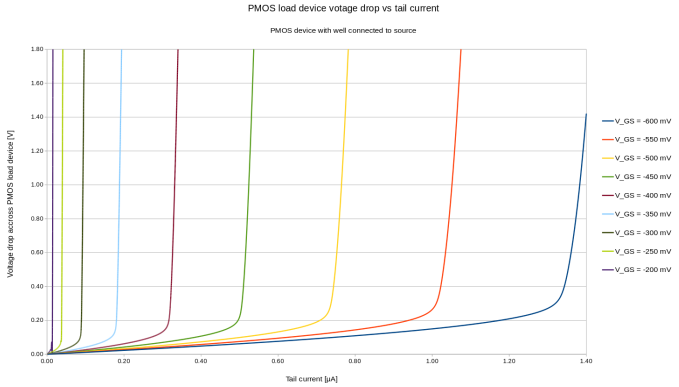


Figure 7: Voltage across a PMOS load device with the well connected to the source, W = 350 nm, L = 10 $\mu$m.

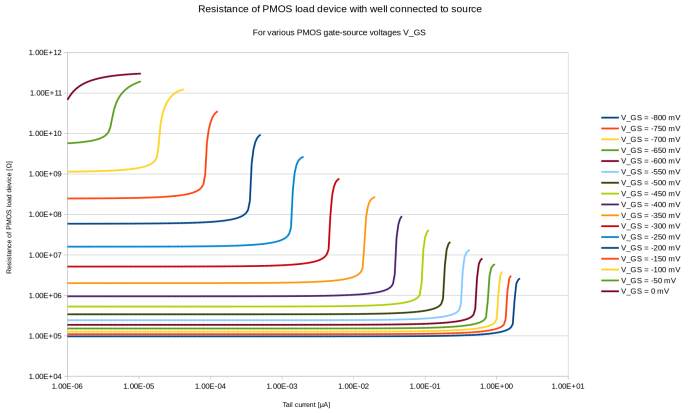


Figure 8: Resistance of a PMOS load device with the well connected to the source, W = 350 nm, L = 10 $\mu$m.

The nonlinear relationship $V_{SD,sat} \propto \sqrt{I_{D,sat}}$, equation 7, implies that it will be difficult to operate the gate with such a load device over a wide dynamic range of tail currents. Figure 7 additionally shows how low the achievable voltage drop $V_{SD,sat}$ is for a reasonably sized transistor in the triode region. In order to achieve in the triode region a sufficient voltage swing we would need a slim and very long transistor. It is unlikely that we will find an acceptable size for the transistor in order to obtain a desired output swing in triode regime. Operating the transistor in saturation is also

not possible, since the differential resistance, see eq. 8, is very high as can be seen on figure 7. In this case the tail current would have to be set very precisely to obtain a well defined output voltage swing.

$$r_o = \frac{1}{\lambda I_{D,sat}} \tag{8}$$

Operating the PMOS load device with the well connected to the source becomes even more of a problem if we tried to operate it with a tail current bellow the threshold current (the current flowing through the transistor when the gate source voltage is equal or bellow to the threshold voltage). In that case the differential output resistance rises into the TΩ range. Equation

$$I_D = I_{D0} \cdot \frac{W}{L} \cdot e^{\frac{q(V_{SG}-V_{THP})}{n_p \cdot kT}} \tag{9}$$

describes the transistor in subthreshold regime and it is accurate as long as $V_{SD} > 4U_T$ or approx. 100 mV at room temperature, where $U_T$ is the thermal voltage. The equation is very similar to the Shockley diode equation, since the transistor is in weak inversion, it is more or less just a reverse biased diode. Equation 9 does not contain the term $V_{SD}$ implying, that the drain current is independent of applied source drain voltage and therefore it is impossible to control the output voltage swing.

From the above stated reasons it follows, that the resistance of the PMOS load device of situation (B) is either to low or to high. This is where the work of Armin Tajalli and Yusuf Leblebici [2] comes into the picture, they connected the PMOS devices with their well connected with the drain instead of with the source, situation (C) on figure 2. This is a rather uncommon structure in CMOS design. Figures 9 and 10 display the I-V curve and resistance of such a PMOS load device. The load devices behave like resistors over a very wide dynamic range with a reasonable linearity. The sensitivity towards the gate-source voltage is also in a range, which makes it easy to correctly bias such devices via feedback. The output swing is limited to 400 mV by the source-bulk diode, which under no circumstances should be opened during normal operation, more on latchup in section 5.8.

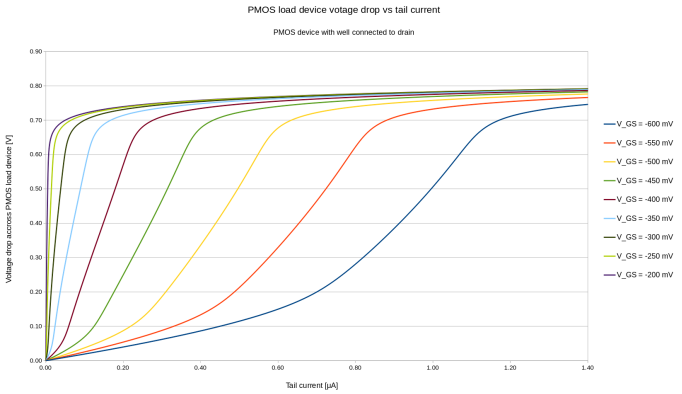


Figure 9: Voltage across a PMOS load device with the well connected to the drain, W = 500 nm, L = 1 $\mu$m.

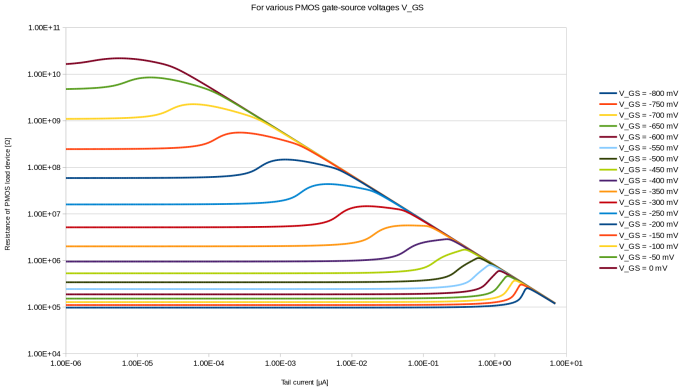


Figure 10: Resistance of a PMOS load device with the well connected to the drain, W = 500 nm, L = 1 $\mu$m.

Whereas the tail current in standard SCL logic is relatively high, in the range above multiple $\mu$A, with STSCL it is possible to reduce the tail current down to right above the leakage current of the transistors in the range of a few pA per gate. This is possible because, contrary to SCL logic, in STSCL the load resistances are feedback controlled and can be set from a few tens of k$\Omega$ up into the T$\Omega$ range. Having the gate operating on such minuscule tail currents means that the maximum achievable clock speeds will be just in the range of a few hundred Hz for the minimum tail current.

To mathematically model the behavior of the load device we will use the EKV PMOS model [6]. The following derivation can be found in [3].

$$I_{DS} \approx 2n_p\mu_p C_{ox}\frac{W}{L_e}U_T^2 e^{\frac{V_{BG}-V_{THP}}{n_p U_T}}\left(e^{-\frac{V_{BS}}{U_T}} - e^{-\frac{V_{BD}}{U_T}}\right) \tag{10}$$

where

- $C_{ox}$ is the gate oxide capacitance per unit area,
- $\mu_p$ is the hole mobility,
- $U_T$ is the thermal voltage,
- $W$ is the transistor width,
- $L_e$ is the effective transistor length,
- $V_{BG}$ is the n-well to gate voltage,
- $V_{BS}$ is the n-well to source voltage,
- $V_{BD}$ is the n-well to drain voltage,
- $V_{THP}$ is the threshold voltage for the PMOS device,
- $n_p$ is the threshold slope for the PMOS device.

For the bulk-drain connected PMOS load device, the voltage $V_{DB} = 0$ we obtain

$$I_{SD} \approx I_0 \cdot e^{\frac{V_{DG}-V_{THP}}{n_p U_T}}\left(e^{-\frac{V_{DS}}{U_T}} - 1\right) \tag{11}$$

where

$$I_0 = 2n_p\mu_p C_{ox}\frac{W}{L_e}U_T^2 \tag{12}$$

We can now calculate the small signal output resistance of the load device as

$$R_{SD} = \left(\frac{\partial I_{SD}}{\partial V_{SD}}\right)^{-1} \tag{13}$$

In equation 11 we can rewrite $V_{DG}$ as $V_{DS} - V_{GS}$ and then perform the derivative of $I_{SD}$ by $V_{SD}$. We obtain

$$R_{SD} = \frac{n_p U_T}{I_0 \cdot e^{\frac{V_{SG}-V_{THP}}{n_p U_T}}} \left( (n_p - 1) \cdot e^{(n_p-1)\frac{V_{SD}}{n_p U_T}} - e^{-\frac{V_{SD}}{n_p U_T}} \right)^{-1} \tag{14}$$

We rearrange and obtain for resistance of the load device

$$R_{SD} = \frac{n_p U_T}{I_{SD}} \cdot \frac{e^{V_{SD}/U_T} - 1}{(n_p - 1)\, e^{V_{SD}/U_T} + 1} \tag{15}$$

## 5.2 Input-output transfer voltage

If the gate is operated in sub threshold regime it can be shown that the transconductance of the input differential pair is [3]:

$$G_m = \frac{\partial I_{out}}{\partial V_{in}} = \left( \frac{I_{Tail}}{2 n_n U_T} \right) \cdot \frac{1}{\cosh^2(V_{in}/(2 n_n U_T))} \tag{16}$$

Voltage gain of the STSCL gate can be obtained by combining equation 15 with equation 16

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = \frac{\partial V_{out}}{\partial I_{SD}} \frac{\partial I_{SD}}{\partial V_{in}} = R_{SD} \cdot G_m \tag{17}$$

Since we are interested in the maximum voltage gain, which occurs for $V_{IN} = 0V$ we can derive

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} \leq A_v|_{V_{IN}=0} \approx \frac{n_p}{n_n \cdot (n_p - 1)} \tag{18}$$

Notice that voltage gain is independent of transistor dimensions, which means that we cannot select an arbitrary gain of the gate. The gain is dependent upon the subthreshold slopes, which are not under the designers control.

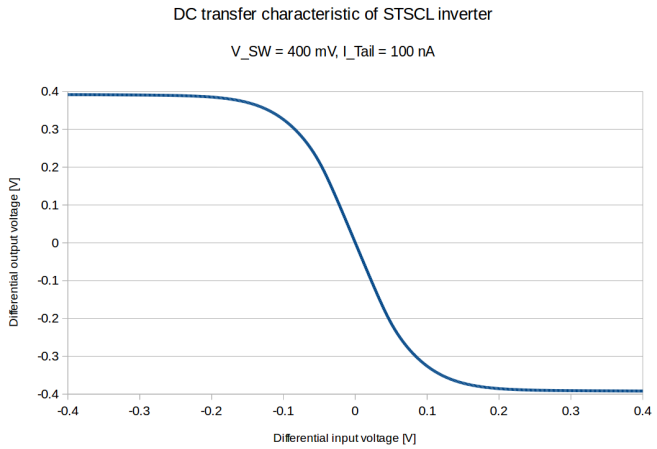


Figure 11: STSCL inverter gate DC transfer characteristic.

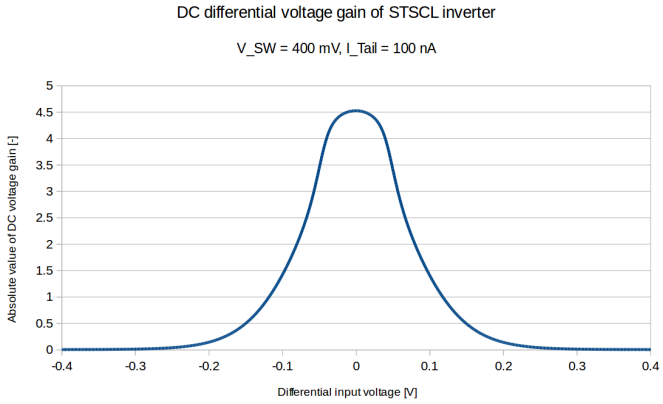


Figure 12: STSCL inverter gate differential gain.

The effect of mismatch effects and process variation can be seen on figures 13 and 14. As can be seen due to the feedback driven architecture of the PMOS load device biasing, the process variation is almost negligible. The mismatch variation has a major effect upon the effective switching voltage swing and the actual noise margin will thus be lower than estimated from the nominal (drawn) gate DC transfer characteristic.

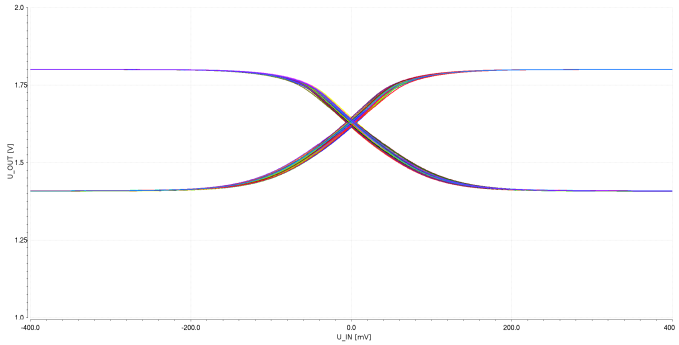


Figure 13: STSCL inverter gate DC transfer characteristic Monte Carlo simulation, process variation only.

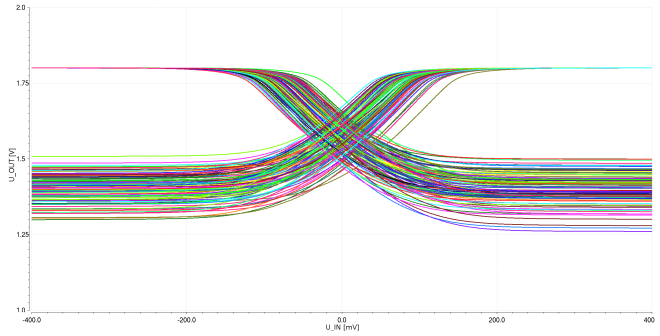


Figure 14: STSCL inverter gate DC transfer characteristic Monte Carlo simulation, mismatch variation only.

## 5.3 Propagation delay

The propagation delay is determined by the parasitic capacitance $C_{out}$ seen by the gate output, the amount of tail current $I_{Tail}$ and the set voltage swing $V_{sw}$. The time constant of an

$$\tau_{gate} = R_L \cdot C_L \approx \frac{V_{sw}}{I_{Tail}} \cdot C_{out} \tag{19}$$

Since the propagation delay is usually defined as the time required for the output to reach 50 % of its final output level and the time constant is defined as reaching $1 - 1/e$ of its final output level, we need to change the base of the logarithm by multiplying by $\ln 2$

$$t_d \approx \ln 2 \cdot \frac{V_{sw}}{I_{Tail}} \cdot C_{out} \tag{20}$$

Both the $V_{sw}$ and $I_{Tail}$ parameters are adjustable in the circuit and can be theoretically used to influence the propagation delay and therefore the speed of the gates. In practice $V_{sw}$ is usually used to set the desired noise margin (is given) and $I_{Tail}$ is used to influence the propagation delay and thus maximum toggling speed. The $C_{out}$ parameter is the only parameter affected by process and mismatch variations. The combined process and mismatch variation for the $C_{out}$ capacitance in the AMS 180 nm process is around 10% (this number does not account for the variation of parasitic capacitance in metal stack, only the transistor capacitances are accounted for in weak inversion). Note that the propagation delay is not affected by the supply voltage.

## 5.4 Tail current circuitry and leakage current reduction techniques

The tail current bias source is realized with two NMOS transistors stacked over each other. The stacking of the NMOS devices was done in order to increase the output resistance of the tail current source in the case of operating the gates close to, or slightly above, the threshold regime (e.g. to run the gates at high clock speeds).

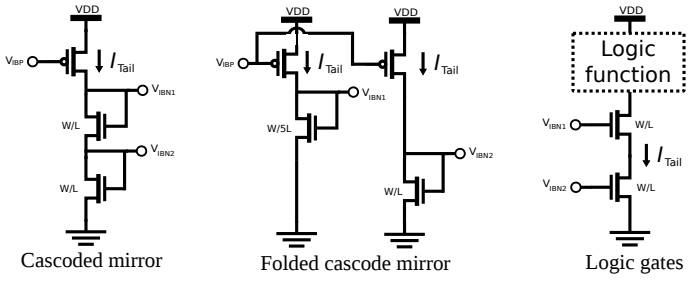


Figure 15: Tail current source circuit and bias circuits to drive the stacked NMOS transistors. Note the folded cascode mirror is only meant for gates biased at or above threshold.

The output resistance of the transistors is strongly dependent upon operating regime. In the sub threshold regime, as long as $V_{DS} > 4U_T$ where

$U_T$ represents the thermal voltage, the output resistance is in the GΩ range and one transistor alone provides a sufficient high resistance, behaving like an ideal current source. Since we work in a deep sub-micron process and will use the smallest possible transistors we must assume short channel effects to affect the transistor behavior. If a minimum length transistor is operated in saturation the output resistance drops into the range of a hundreds of KΩ or even less. In very low noise applications is desirable to have a higher output resistance. For a single MOSFET transistor the output resistance is [5], p. 288

$$R_{out} \propto \frac{L^2}{V_{DS,sat}^2} \tag{21}$$

If operated in saturation, the cascoded tail current structure from figure 15 displays an output resistance of [5], p. 638

$$R_{out} = (2 + g_m \cdot r_o) r_o \cong g_m \cdot r_o^2 \tag{22}$$

Stacking the transistors is also useful in the case of extreme low power operation (deep subthreshold), where the minimum possible tail current is used. Stacking provides the additional benefit of reducing the leakage current making it possible to operate the circuits with a tail currents in the pA range. Since the PDK transistor models provided by the foundry are omitting many of the various leakage currents present in deep sub micron processes, like for example GIDL (Gate Induced Drain Leakage), the gate oxide tunneling current, punch trough in the substrate, induced substrate currents from the parasitic bipolars etc., it will be necessary to verify the behavior of the STSCL gates at extremely low tail currents through verification by measurement on actual silicon.

The minimum tail current at which the gate can be operated, must be above the leakage currents of the used transistors. It is possible to reduce the leakage current by up to a factor of ten in comparison of a single transistor by stacking transistors as on figure 16.

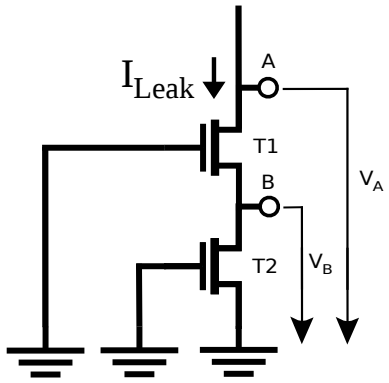


Figure 16: Stacked NMOS transistor current source in off state.

By placing two transistors on top of each other the node B on figure 16 will not be at ground potential, but somewhere between voltage $V_A$ and GND. Since voltage $V_B$ is the source voltage of transistor T1 and since the gate voltage is at ground potential, the gate-source voltage applied to transistor T1 is thus negative. By driving the gate-source voltage negative the subthreshold leakage current can further be reduced exponentially. Since the bulk of the transistor T1 is also tied to ground, the body to source voltage $V_{BS}$ is also negative, which has the effect of depleting the channel further of minority carriers and also contributes to a reduction of leakage current, see EKV subthreshold equation 23.

$$I_{DS} \approx 2n\mu_e C_{ox} \frac{W}{L_e} U_T^2 e^{\frac{V_{GB}-V_{THN}}{n_n U_T}} \left( e^{\frac{-V_{SB}}{U_T}} - e^{\frac{-V_{DB}}{U_T}} \right) \tag{23}$$

The impact on design complexity consists mostly of having an additional transistor in the logic gates and another bias rail. Biasing the current tail current source now requires a cascoded current mirror and two bias voltage rails to distribute to the reference voltage to the gates. Since the gates designed in this thesis are to be used with a supply voltage of 1.8 V, driving a cascoded current mirror is not an issue in terms of supply voltage headroom even in the case of of driving the gates into saturation ($V_{supply}$ must be larger than $2V_{THN} + V_{DS,sat}$ where $V_{THN} =\approx 550mV$). Should in the future the request arise to use these gates close to saturation at a lower supply voltage a different bias voltage generator circuit must be used, for example with a folded cascode[5], see figure 15. Note, that the folded cascode circuit is meant for the saturation regime (close to or above threshold ) and not for the deep

subthreshold regime.

## 5.5 Biasing the PMOS load resistors

The tail current can be varied across a very wide dynamic range. The lower limit is given by the leakage current of the used transistors. The upper limit of the tail current is given by the resistance of the PMOS load devices (Note that in STSCL the voltage swing must remain bellow the forward voltage of source-to-well diode since otherwise a parasitic well PNP transistor might be opened, more on the subject of latchup in section 5.8). The maximum possible tail current is already set during the design phase by choosing the width of the PMOS load devices.

The resistance of the PMOS load resistors is determined by the applied gate source voltage. If the PMOS device is operating in the subthreshold regime there is an exponential relationship between the the applied bias voltage on the gate and the current flowing through the PMOS device. The resistance of the PMOS device can be adjusted in a very wide dynamic range. The question now arises which bias voltage to chose? The answer is that the voltage will be derived with help of a special feedback circuit [2]. The bias voltage will be derived by placing a dummy PMOS load device and pulling the desired tail current trough it. An differential amplifier will monitor the drain voltage of that PMOS device and compare that voltage with an external reference voltage. The differential amplifier adjusts the PMOS load device gate source voltage until the drain voltage for the given tail current equals to the preset reference voltage. This gate voltage is then distributed to all STSCL gates operating with the given tail current. With this circuit it is possible to dynamically adjust the voltage swing of the STSCL cells.

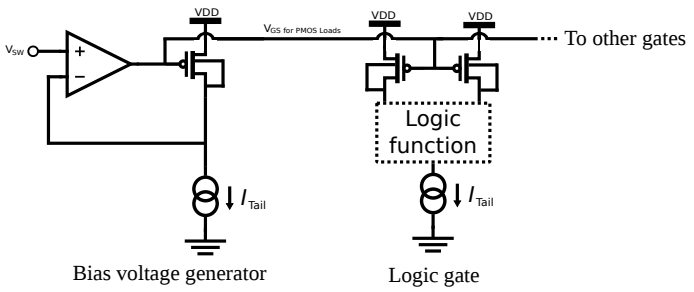


Figure 17: The schematic of the final bias circuit cell.

The voltage swing should always be limited to less than 500 mV to prevent the parasitic PNP transistors from opening. Reducing the STSCL voltage swing has the effect of increasing the maximum switching speed for a given tail current, but at the price of a reduced noise margin. The save operating region for the voltage swing is between 200 mV and 400 mV.

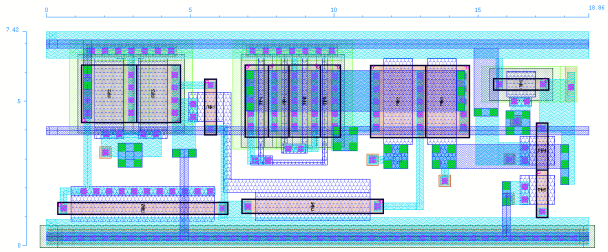

Figure 18: The layout of the final bias circuit cell.

## 5.6 Noise margin

The noise margin of a logic gate is a measure of how much the input signal can be distorted by noise from its steady state amplitude, before the logic gate starts to react on its output to that input noise. It is a measure of the robustness of digital circuits against noise perturbations on the signal lines before transients, logic hazards and accidentally toggled flip-flops occur. There are various criteria by which one can chose to quantify the static noise margin of logic circuits. An excellent overview of the concept of a static noise margin is given in [7]. A logic gate is a highly nonlinear circuit. It is this nonlinearity, what makes logic circuits resilient against noise. As was shown in section 5.2, the gain of a STSCL gate reaches its peak value around a zero differential input voltage and rapidly rolls off as the circuit reaches saturation. In the state of saturation the whole tail current is flowing only through one branch of the two load PMOS devices. In saturation small changes in the input voltage do not produce any changes of the output voltage. The gate blocks all noise to a certain threshold - a fundamental and desired property of digital circuits. If the differential input voltage of the gate is far enough from the steady state voltage such that the gain raises above one, then the

gate will amplify the noise distortion and the noise signal can pass to the next gate where it might get amplified even more and so on. A cascade of errors can then spread through the digital circuit. If a perturbation occurs on a digital signal line, such that the voltage level remains in the interval defined by the noise margin, then the perturbation will occur on the output of the gate attenuated and cannot spread throughout the digital circuit. There are various noise sources affecting digital circuits and each has its own associated noise margin. Among the various noise sources one needs to consider the series voltage noise on the logic lines $\Delta V_{series}$, parallel current noise $\Delta I_{parallel}$ and noise on the power rails $\Delta V_{vdd}$ and $\Delta V_{gnd}$ among others. In this work only the series voltage noise on the logic lines $\Delta V_{series}$ was analyzed since in STSCL circuits the condition that $R_{out} \ll R_{in}$ is usually fulfilled and thus the parallel noise is negligible and noise injection through the power rails is strongly suppressed by isolation provided by the presence of the tail bias current source.

In this work the worst case static noise margin will be defined as the maximum square between the normal and the mirrored voltage transfer characteristic. It is a geometric definition. To better illustrate see the schematic on figure 19.

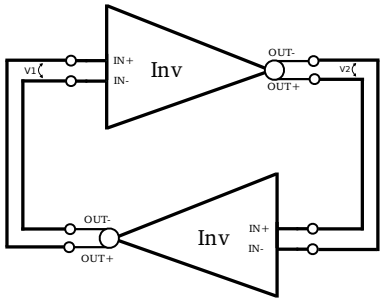


Figure 19: The circuit used to quantify the noise margin.

The circuit on figure 19 is a bistable circuit of two inverters connect in a loop. There are two differential voltage nodes V1 and V2 in this circuit. Let us assume that this circuit is in a given logical state; for example V1 is in a logical '0' and V2 is a logic '1'. The circuit is exposed to series noise which is added to the logic nodes V1 and V2. We are interested in the worst case noise voltage $\Delta V_{series}$, which can be added to the voltage of node V1 and at the same time subtracted from the voltage at the node V2, such that the

circuit does not become metastable.

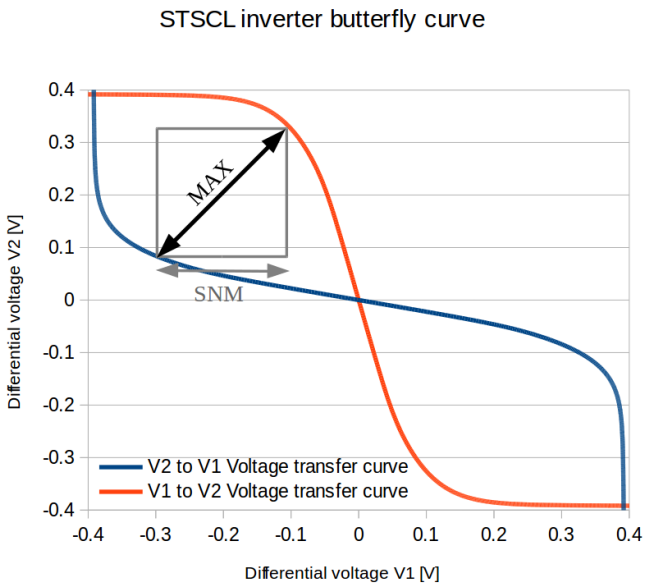


Figure 20: The butterfly curve for the designed STSCL inverter with the geometric definition of the worst static case noise margin displayed.

Figure 20 displays the so called butterfly curve for the circuit from figure 19. It shows the two voltage transfer characteristics of the two inverters, but each on a different axis. Adding series voltage noise has the effect of shifting the voltage transfer characteristic to the left or right; resp. up or down. If we for example add a certain amount of noise $\Delta V_{series}$ to the voltage V1, we shift the orange curve downwards. If we subtract a certain amount of noise $\Delta V_{series}$ from the voltage V2, we shift the blue curve right. The worst case series voltage noise margin can be found geometrically by determining the largest possible square which fits between the normal and the mirrored voltage transfer characteristics. If we shift both transfer characteristics by this static noise margin value (SNM) they will barely touch in the corner of the square and metastability arises. It is shown in [7] that this geometric definition is equivalent to stating that the loop gain of the circuit from figure 19 has risen above one.

The mathematical expression for the worst-case noise margin of a subthreshold SCL circuit is given by [3]:

$$NM_{STSCL} = V_{SW}\left(\sqrt{1-\frac{1}{A_V}} - \frac{1}{A_V}\cdot tanh^{-1}\left(\sqrt{1-\frac{1}{A_V}}\right)\right) \qquad (24)$$

where $A_V$ is the maximum DC voltage gain of the gate, see section 5.2. Since the sub threshold DC voltage gain $A_V$ cannot be influenced by choice of transistor dimensions, see equation 17, the only way how to set the noise margin is by choosing a sufficiently high voltage swing $V_{SW}$. The voltage swing $V_{SW}$ is feedback controlled, see section 5.5, and can be set from $0mV$ to around $500mV$ before the parasitic source diode of the load PMOS transistor opens. If we wish to reduce $V_{SW}$ for example in order to speed up the digital circuit, our noise margin will fall linearly with the reduced $V_{SW}$. Equation 24 predicts for the designed STSCL circuits (gain $A_v = 4.5$) a noise margin of 57% of the switching voltage $V_{SW}$, or $NM_{STSCL} = 228mV$ at $V_{SW} = 400mV$. The graphical method from figure 20 suggests a worst case static series noise margin of $NM_{STSCL} \approx 230mV$. The designed logic gates have a symmetrical noise margin for both logic levels.

## 5.7 Fanout and drive strength

The logic gates developed in the scope of this work are not intended for general purpose digital circuits, but for very special low noise digital IP blocks to be used in ultra low noise measuring ASICs for nuclear detectors. It is envisioned that the gates will be used in the analog design flow (Virtuoso) and not in the digital design flow (Encounter). It is currently not anticipated that the gates will be used in complex digital circuits, but rather in tinny digital IP blocks performing simple functions close to the analog front end. The correct function and the meeting of timing constraints present in such IP blocks must be verified by transistor level transient simulations and post layout simulations. Just one drive strength was implemented for each type of gate, which limits the possible fanout. The drive strength of an STSCL gate is given by its tail current. It is possible to modify the tail current from cell to cell by adjusting the transistor sizes of the tail current biasing structure. By making this transistor twice the the tail current will be doubled. By doubling the length of the transistor the tail current can be halved. This method of creating gates with various drive strengths has the advantage that the cells can be placed in the same bias rails, but has the disadvantage that the PMOS

load resistances are being set for one given tail current and modifying the tail current affects the voltage swing on the gate output.

## 5.8 Latchup protection

In STSCL the n-well of the PMOS load devices is connected with the drain instead of the source as is it is with PMOS devices normally the case. Having the n-well not at the same potential as the source carries the risk, that the parasitic back-gate transistor might be opened if the well voltage drops bellow the supply voltage by more than 500 mV. Latchup itself does not directly occur in this case since the base of the parasitic PNP transistor is connected to a current source (the STSCL tail current) and thus the current flowing from the source (emitter) into the substrate is limited. If the substrate around the PMOS load device has insufficient ground contacts nearby, the small current flowing into the substrate from the transistor n-well might rise locally the substrate voltage and open a parasitic NPN transistor. A parasitic NPN transistor is present if a NMOS device is nearby the PMOS transistor. Once the NPN is open the current is not anymore limited by the tail current. Once the parasitic NPN transistor is open latchup occurs. It is usually not good practice to open the parasitic PNP transistor inherently present in each PMOS device. Analysis via simulation of the severity of this issue was not possible during the design phase since the parasitic bipolar transistors are not being modeled by the technology PDK.

Even if latchup does not occur, the current flowing into the substrate can be substantial risk since the parasitic PNP transistor is of the vertical type and can have a significant current gain. It was not possible to obtain estimates of the current gain of the parasitic bipolars from the foundry. The current gain of the parasitic bipolar devices is not documented in the process PDK and must be determined either through measurement or with a TCAD simulation. Determining the current gain is outside the scope of this work.

A few simple steps were undertaken during the design phase to reduce the risk latchup in STSCL circuits:

- Partial guard-rings tied to GND around the PMOS load devices to collect accidental substrate currents from the PNP transistor.
- Add a pull up protection diode in front of the $V_{SW}$ bias circuit. The pull up diode will prevent accidentally setting the N-well voltage to low and forward biasing the base junction of the parasitic PNP transistor.

- The tail current is set not with a current steering DAC, but with a voltage DAC projected though a transconductor. The transconductor resistor is chosen such that the maximum accidental supply current is limited to value that can be handled by the wire-bonds and does not exceed the value set by electro migration requirements. This limits the maximum current in the case of single event upsets in the configuration registers.

- The configuration registers flip flops have a safe initial default value and are not initialized randomly after power-up.

Figure 21 displays the schematic of a simple transconductor circuit used to set the tail current. It has the advantage that the maximum tail current is well defined by the resistor and the supply voltage.

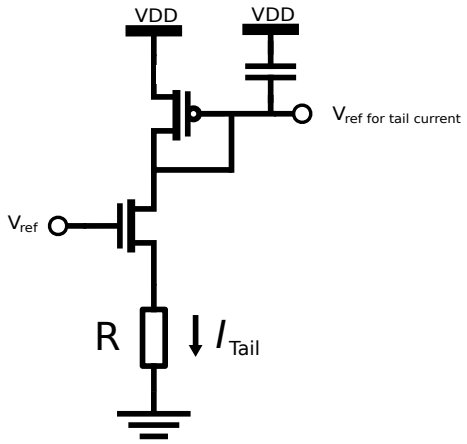


Figure 21: The schematic of the fail-safe current limiting tansconductor.

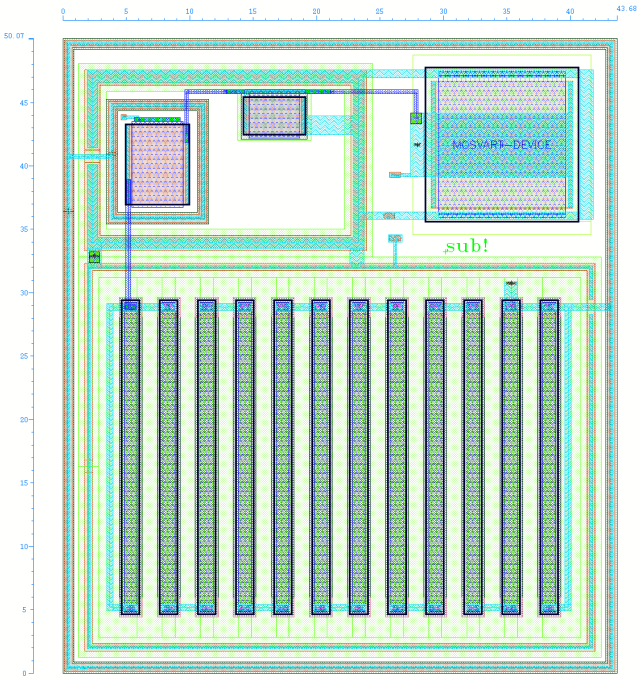


Figure 22: The layout of the fail-safe current limiting tansconductor.

## 5.9 Layout considerations

Standard CMOS logic gates need two power rails, the STSCL gates need the two power rails and additionally two (three) bias rails. When a designer routes a STSCL circuit the high density metal routing becomes very quickly an issue since each logic signal consists of two physical wires. The interconnect density is further increased by the fact that in STSCL every gate usually performs two functions at the same time (inverter is equal to buffer, OR is equal to NOR etc.) This means that a given circuit synthesized into STSCL gates uses fewer gates than a circuit synthesized into CMOS gates. The initial intuitive assumption, that because STSCL gates have more transistors and thus the layout must be larger than in CMOS is wrong. The larger size of the STSCL gates is more than compensated by the fact that fewer gates are necessary for a given function. The actual reason why a circuit realized in STSCL might turn out to be larger than the equivalent CMOS circuit is that the wiring density necessitates the insertion of filler cells.

In this particular STSCL realization on the AMS 180 nm process node, 6

metal layers are available, but the sixth metal layer is a low precision thick metal layer, useful only for power distribution and not signal transfer.

Routing the gates into the final circuit is the main difficulty in taping out a STSCL IP cell. A designer can significantly simplify his life of routing the netlist, by putting a lot of time into the layout design at the gate hierarchical level. The cells must be buttable - by placing two cells next to each other, the power rails and the bias rails should automatically be interconnected, and should not have to be routed by hand. The cells should also have the input pins on one side and the output pins on the other side. The pins should be well accessible on the highest metal layer used to route the gate.

Another important feature in STSCL layout is the consideration of threshold matching. STSCL gates contain current mirrors and hence the threshold voltage must precisely controlled during manufacture. In standard CMOS logic circuits the threshold variation is not so important for the correct functionality of the circuit. The transistors in the STSCL gates should have the analog DRC ruleset applied to them. The final threshold of transistors is affected by antenna charging effects during plasma etching of metal layers. Even though the charging of exposed metal surfaces is insufficient to cause gate breakdown, the high electric field together with elevated temperatures might shift the transistor threshold and worsen mismatch effects. In modern CMOS processes digital circuits have lesser stringent antenna DRC rules than analog circuits and the standard cell gates provided by the foundry have a special layer marking them as digital circuits in the design rule check. Having the STSCL gates not marked as digital circuits will mean that antenna rule violations will be a severe issue when routing the netlist hierarchical level, unless the the antenna effects were already considered during gate design phase. The mitigation strategy for this effect is, that the lowest metal gate connections, which do not have a substrate tap (connected to the drain or source of another transistor) on the same metal level within the gate a tie down diode must be placed on this metal layer. These tie down diodes should be added early in the design phase since they will increase the gate input capacitance and they will consume a bit of silicon area inside the gate layout. Since STSCL consumes a constant current, the supply rings around IP blocks as done typically for CMOS can be omitted or their size can be reduced significantly. Supply voltage rails can be designed thinner, than is usually done for the equivalent CMOS circuits since the CMOS version must be designed for the peak current to reduce voltage spikes on the power rails and meet electro migration rules.

## 5.10 Interfacing STSCL to standard CMOS logic

Not always are STSCL gates the best option. Low rate logic circuits like configuration bits or logic circuit which are only active at times, when noise is not a critical issue can realized in CMOS logic. For example nuclear detector readout ASICs are either acquiring data ( shutter on, low noise operation is required), or the collected data are being extracted by an external data acquisition system (shutter is off, noise is irrelevant). The digital circuits, that implement the logic glue for transferring the data out of the chip are best implemented in standard CMOS (easier routing, ergonomic design flow). Static digital circuits which serve the function of setting configuration bits are also best implemented as CMOS, since STSCL would cause unnecessary power consumption in the static regime. This suggests that in a final chip design a combination of STSCL and CMOS digital circuits will be present and it will be necessary that they communicate between one another.

If the logic signal path is not time critical, it is possible to directly realize the signal flow from the CMOS domain into the STSCL domain. An inverted, complementary signal of the CMOS signal must be produced and that differential CMOS signal can then directly drive a STSCL gate. The differential signal will not be perfect in the sense that the inverter will introduce a delay and thus there will be a phase shift between the two CMOS signals.

A second variant to transfer a CMOS signal into the STSCL domain is using a static reference voltage instead of an inverter for the complementary STSCL input. This topology is suitable for high speed interfaces. A disadvantage of this approach is that the CMOS signal has a nonzero rise/fall time and that the method of using a reference voltage for the complementary STSCL input can affect the duty cycle. It is advisable to place a CMOS buffer for the CMOS signal directly in front of the receiving STSCL element, in order to ensure the maximum possible rise/fall time. The reference voltage can be chosen half the CMOS supply voltage and can be generated with a simple resistor divider.

The connection from the STSCL logic domain into CMOS domain is more challenging. In this case a level shifter is a must, since the STSCL $V_{OL}$ level is far above the CMOS $V_{IL\,max}$ level. Many level shifter topologies are possible here. An example level shifter topology can be seen on figure 23 and figure 24. This level shifter has the disadvantage of having a static power consumption equivalent to three STSCL gates, but the logic output signal is

rail to rail.

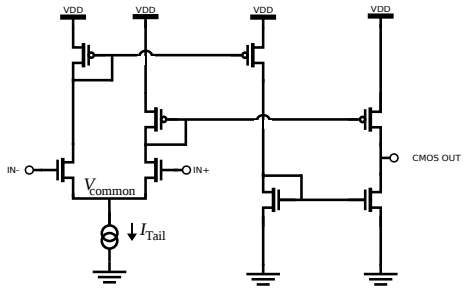


Figure 23: Schematic the voltage level translator used to convert STSCL to CMOS logic levels.

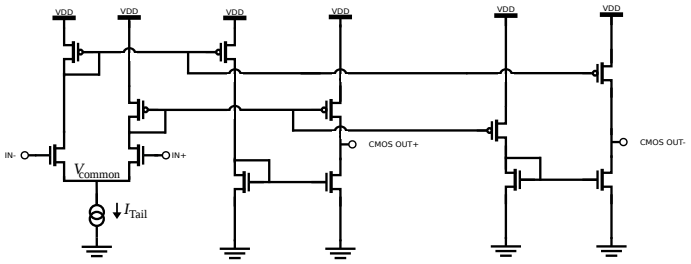


Figure 24: Schematic the voltage level translator used to convert STSCL to complementary CMOS logic levels.

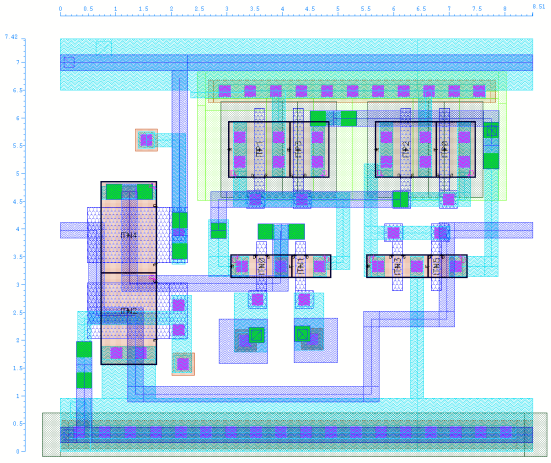

Figure 25: Layout the voltage level translator used to convert STSCL to CMOS logic levels.

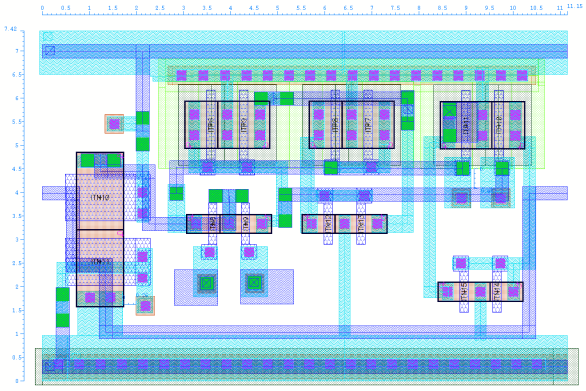

Figure 26: Layout the voltage level translator used to convert STSCL to complementary CMOS logic levels.

# 6 The logic library

The STSCL library developed contains all necessary gates commonly encountered in digital design. Due to the differential nature of the gates each cell represents automatically its complementary function. An "inverter" connected to the output of any gate is easily implemented by swapping the positive with the negative terminal of the differential output. Each gate thus can perform two logic functions. For example a buffer and inverter are one and the same gate in STSCL, but two separate gates in CMOS. The choice which function is realized by the gate depends upon the assignment of the gate output.

## 6.1 The STSCL inverter/buffer

The simplest logic gate is the inverter/buffer. Figure 28 displays the schematic of the designed inverter.

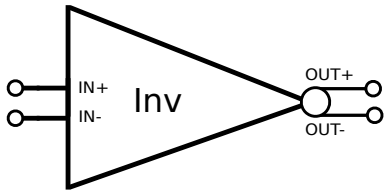


Figure 27: Schematic symbol of a STSCL inverter.

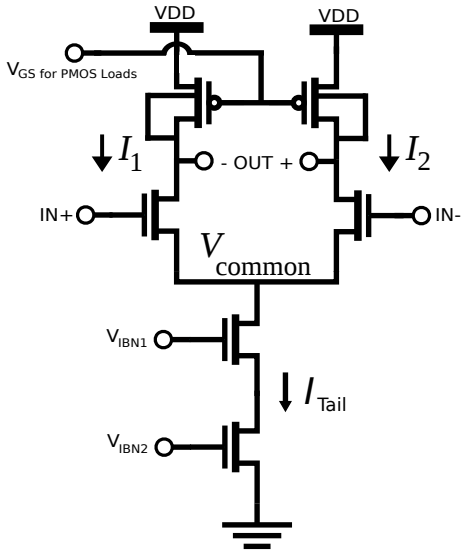


Figure 28: Schematic of a STSCL inverter.

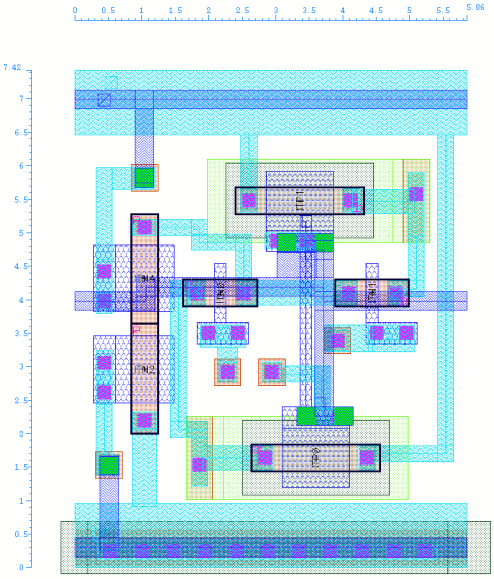

Figure 29: Layout of the designed STSCL inverter.

## 6.2 The STSCL AND/NAND gate

The NAND/NOR gate the is limited to two inputs. Implementing nands with more inputs is complicated by the fact that many transistors need to stacked on top of each other. The fan-in is limited to two or three.

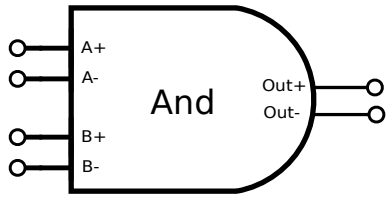


Figure 30: Schematic symbol of a STSCL AND/NAND gate.

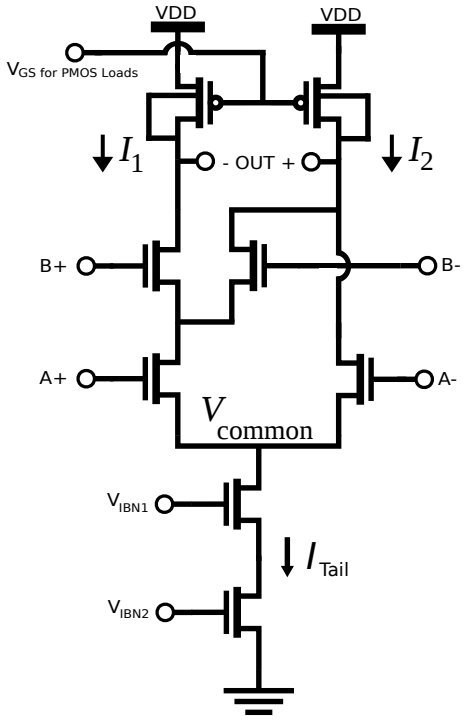


Figure 31: Schematic of a STSCL AND/NAND gate.

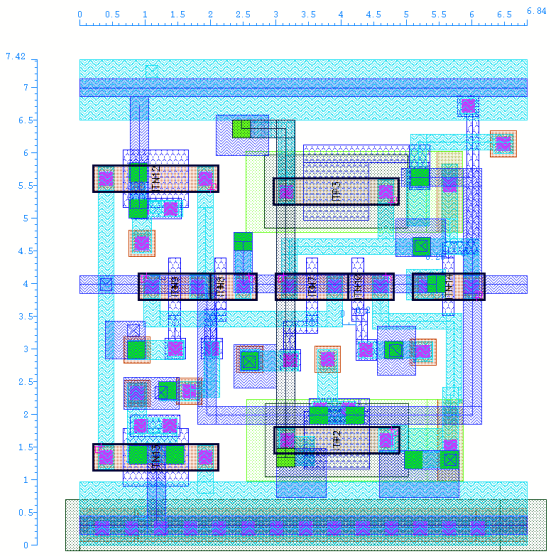

Figure 32: Layout of the designed STSCL AND/NAND gate.

## 6.3 The STSCL OR/NOR gate

The OR/NOR gate is structurally the same as the AND/NAND gate, just the assignment of the input pins has changed.

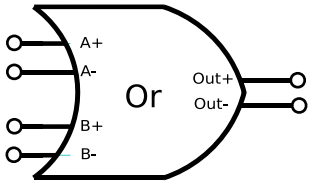


Figure 33: Schematic symbol of a STSCL OR/NOR gate.

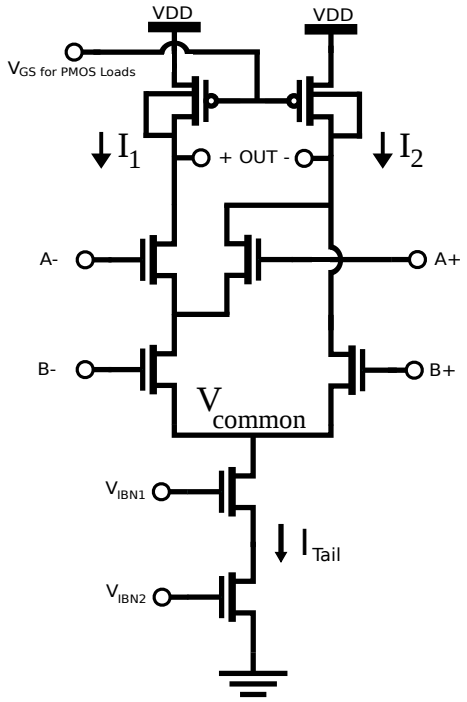


Figure 34: Schematic of a STSCL OR/NOR gate.

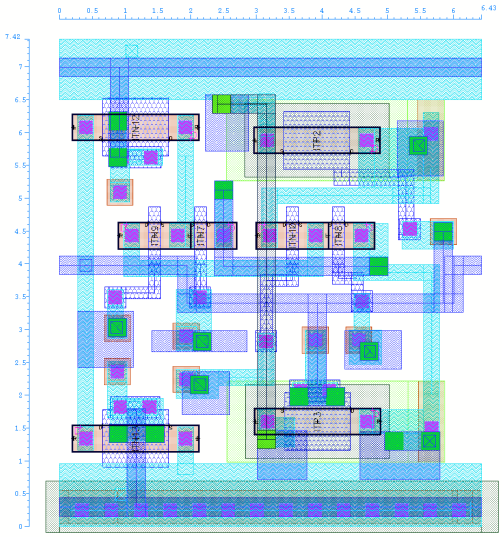

Figure 35: Layout of the designed STSCL OR/NOR gate.

## 6.4 The STSCL XOR/XNOR gate

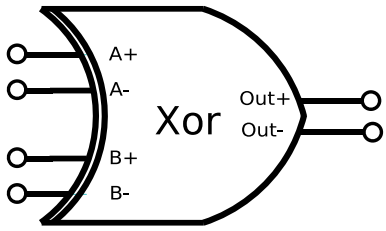


Figure 36: Schematic symbol of a STSCL XOR/XNOR gate.

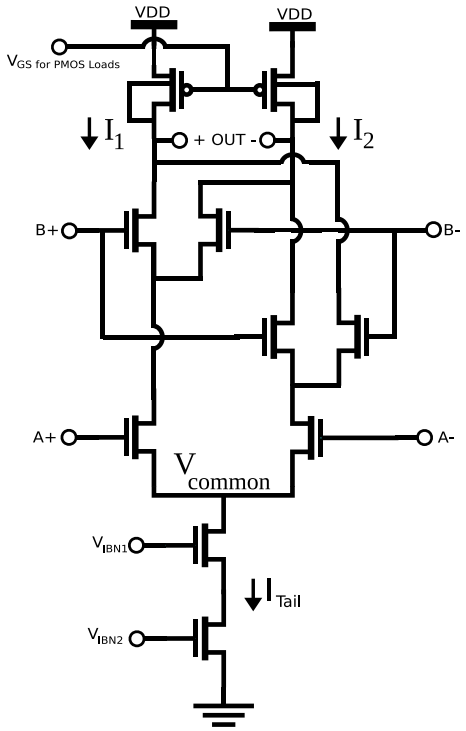


Figure 37: Schematic of a STSCL XOR/XNOR gate.

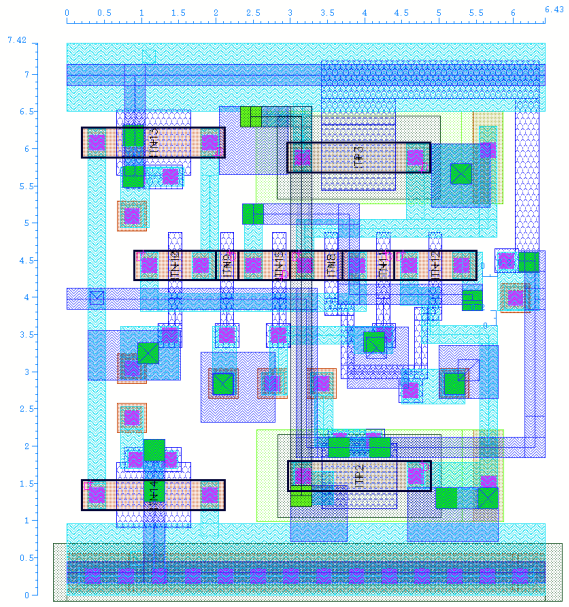

Figure 38: Layout of the designed STSCL XOR/XNOR gate.

## 6.5 The STSCL D-Latch gate

The D-latch gate utilizes a two cross-coupled transistor pairs. The first one, transistors with the D+ and D- pins attached to their gates form the so called sense pair. If the enable input (E+ and E-) is active all the tail current is driven trough the sense pair and the input appears on the output of the gate. The output capacity is charged to the given input signal. The second transistor pair, the transistors next to the reset transistor, form the memory pair. The memory transistor pair senses the output of the D-latch gate. While the enable input is active the second transistor pair is inactive (no current flowing), when the enable goes from active to inactive the first transistor pair is disabled and the second pair locks the output signal.

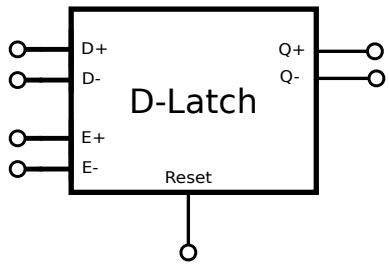


Figure 39: Schematic symbol of a STSCL D-Latch gate.

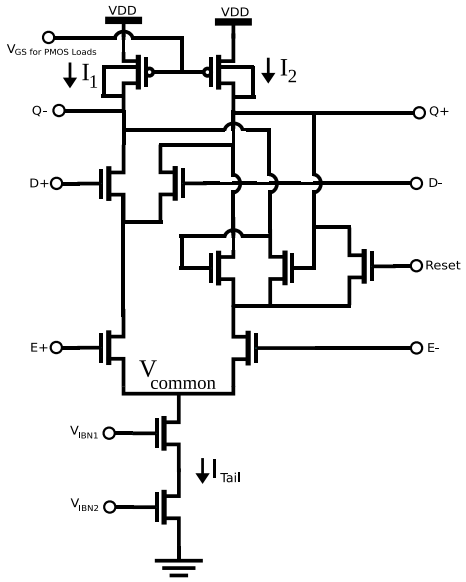


Figure 40: Schematic of a STSCL D-Latch gate.

Additionally a reset signal is present (transistor with Reset pin attached to gate). It is used to set the D latch into a known state independently of the D input signal. The reset signal is a single ended CMOS signal. The reset signal is functionally used to set the IP block into a known initial state. It is usually an asynchronous high fanout signal with a slow slew rate. By implementing the reset signal as a CMOS signal the routing density was greatly reduced and while losing the ability to use the reset signal dynamically in the circuit logic function. This was acceptable in the desired application.

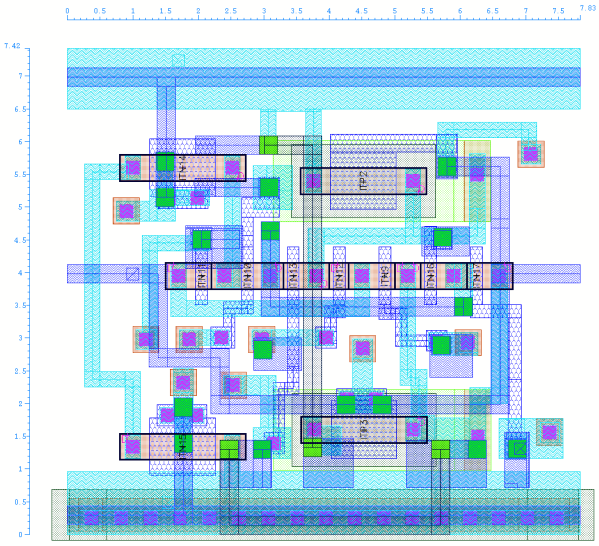

Figure 41: Layout of the designed STSCL D-Latch gate.

## 6.6 The STSCL D flip flop

The D flip flop was designed simply as a master-slave structure made of two interlocked D-latches.

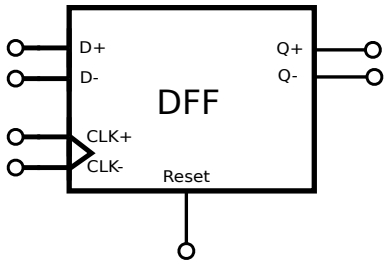


Figure 42: Schematic symbol of a STSCL D flip flop

The schematic of the D flip flop can be seen on figure 43. The D flip flop operates by utilizing both clock levels. When the incoming clock is low, the data on the D input of the flip flop are transfered onto the first D-latch, while the second latch is disabled. One the transition of the clock signal from zero to one the data now present on the first latch output are transfered onto

the second latch of the D flip flop and the input thus appears on the output. While the clock pulse is high the second latch is enabled and senses the first latch, which is disabled and holds the data, that were present when the rising edge of the clock occurred. When the clock signal falls, the second latch is locked and the first latch starts sensing the D input again.

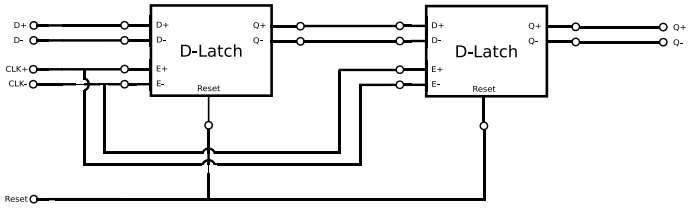


Figure 43: Schematic of a STSCL D flip flop

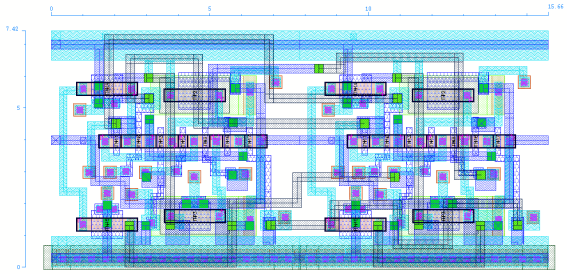

Figure 44: Layout of the designed STSCL D flip flop

## 6.7 The STSCL filler cell

At last, cell that is not obvious, but comes always handy in digital circuit design is a filler decoupling capacitor. Digital circuits seldomly fill out the whole area available due to routing constrains. This is especially true for STSCL circuits due to the increased routing density. The filler cell is used to fill the voids in the circuit layout and can be used to insert decoupling capacitors into the circuit design. It is good practice to have the PMOS load resistor bias voltage decoupled, since this bias rail is capacitively coupled through the drain-gate $C_{gd}$ and bulk-gate $C_{gb}$ parasitic capacitance of the load PMOS devices [5]. Since all STSCL gates always have two load PMOS

devices driven complementary most of the induced charge should cancel out, nonetheless the $V_{SW}$ bias device from section 5.5 has a high impedance output so it cannot compensate the capacitive currents when a large number of STSCL gates switch simultaneously. Figure 45 displays the layout of STSCL filler cell which fits into the STSCL rails. It is a simple PCD MOS capacitor which can be tied to any rail, be it a bias rail or a power rail.

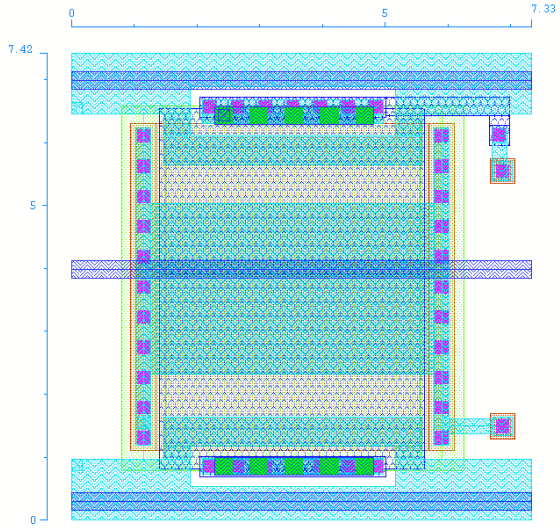


Figure 45: Layout of the designed STSCL filler cell

# 7 Design of a low noise 40 bit STSCL TOA counter

TOA stands for Time Of Arrival. This type of counter is an IP cell used in particle detectors to measure the time interval between the particle hits in the detector. Knowing the exact time of arrival is a feature that is used in precise detectors of ionizing radiation, where charge sharing occurs between multiple sensor channels or where a particle track (simultaneous event in multiple detector channels) needs to be reconstructed. In precise dosimeters, which do not simply integrate the charge from the sensor, each event is

individually measured (the amount of electrical charge from the sensor) and the event is timestamped. With such detailed data (energy and time of event) it is then possible to indicate which radioisotope is the likely source of the ionizing radiation, it is possible to estimate the actual dose received by nearby living organisms, and many nonlinearities of the sensor can be algorithmically corrected. Since the interval between events might be very large, especially in dosimetric applications, the internal counters in the front-end channels could overflow. Having a deep counter in each front end channel is not practical. Having a deep counter implemented in each frontend channel would mean more precious silicon area used and also rise the power consumption of the chip.

In order to nonetheless be able to perform long interval TOA measurements in a low rate environment it was decided to implement an IP cell of a global TOA counter, which there will be only one per detector ASIC. This counter will always be active. After exploring the design possibilities, it became apparent, that such a global TOA counter has many additional valuable use cases:

- It can be used to calibrate the internal ring oscillators. The detector chip contains internal slope ADCs in each channel used to measure the energy of the collected charge. For reasons of simplicity and low power design these slope ADCs are clocked from ring oscillators and not by an precise clock form a PLL. This is not an issue, since the clock frequency must not be exactly set to a certain value. All that is necessary is that the current clock frequency is known to a reasonable high precision. The TOA counter is designed in such a way, that it measures the time length of the shutter window with the internal ring oscillator. Since the shutter window length can be set with high precision by the crystal driven external microcomputer/FPGA it is therefore possible to exactly determine continuously the current frequency of the internal ring oscillator and to remove the effect of frequency drift of the ring oscillator due to temperature changes of the system.

- Another feature is adding a fixed internal delay to the shutter signal. Reading out particle detectors entails the act of measuring extremely small charges in the order of femto Coulomb from sensors with relatively large parasitic capacitances. In order to not add more stray capacitances to the sensor channels the readout chip must be closely

integrated with the sensor diode array. Having an internal delay to the shutter signal is useful in the sense, that it prevents the detector becoming active before all external CMOS signals have settled and thus prevents crosstalk from the digital domain into the analog domain. A common issue observed with detector ASICs is a fake hit caused by the shutter signal. This issue is especially severe in the case when the detector performs a first hit energy measurement. In this mode the detector would measure the charge injected due to cross-coupling of the detector with the shutter signal line and the detector would thus never perform the measurement of an actual particle event.

The above stated considerations were the reason why implementing the global TOA counter in STSCL logic was deemed suitable. The counter is always active and is a high rate (active in each clock cycle) IP cell with well defined timing constraints. Since the counter is always active, when the shutter is open, the low switching noise capabilities of STSCL are very desirable. The cell is sufficiently simple to serve as a test structure.

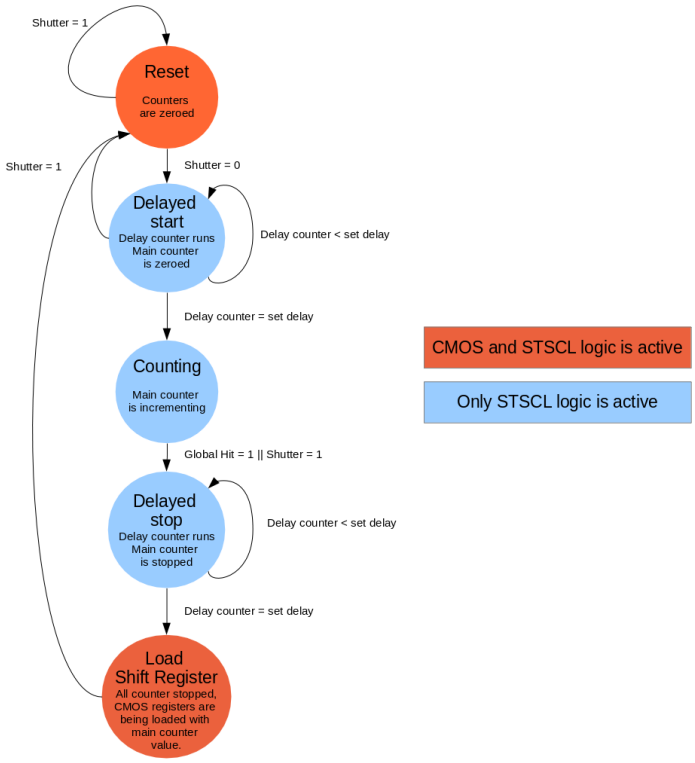


Figure 46: The state diagram depicting the transitions of the TOA 40 bit counter. When the counter exits the first delay it gives an internal shutter signal which can be used by other internal circuitry. The counter stops either on the shutter closing (counter measures the time of the open shutter) or it stops on the first global hit signal (It measures the time of arrival of the first particle.)

The state diagram of the counter finite state machine is depicted on figure 46. As can be seen the counter either measures the time of arrival of the first particle or it measures the time of the shutter window (this information is useful to calibrate the slope ADC ring oscillator used in energy measurement). The start of the internal shutter can be delayed from the external shutter. This feature was desirable, since in our previous experience the shutter signal causes cross talk in the PCB level. The internal delay counter can be configured to be 2048, 4092, 8192 or 16384 clocks of the internal oscillator.

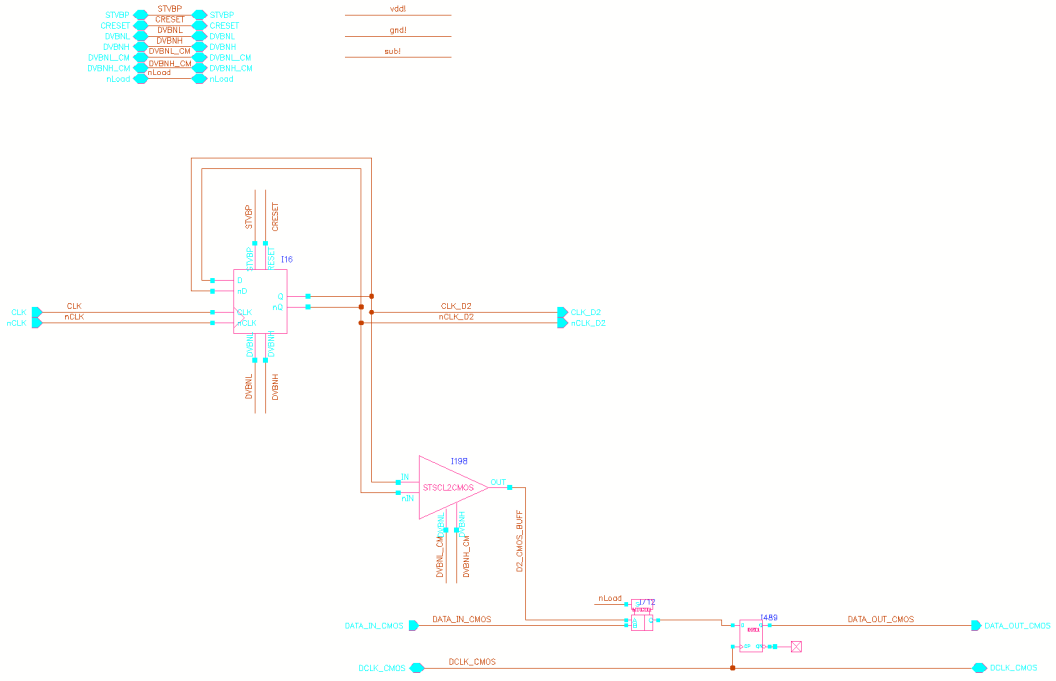


Figure 47: The RTL schematic of a single bit of the final 40 bit TOA counter IP cell. The whole counter consists of 40 such bits connected sequentially plus additional logic glue performing the state space transitions.

The value of the counter is accessible to the external world through a CMOS shift register, which is off-line when the shutter is open and which once the shutter closes will load the final value of the STSCL counter. When the shutter is closed the CMOS shift register can be read out.

Figure 48: The RTL schematic of the final 40 bit TOA counter IP cell.

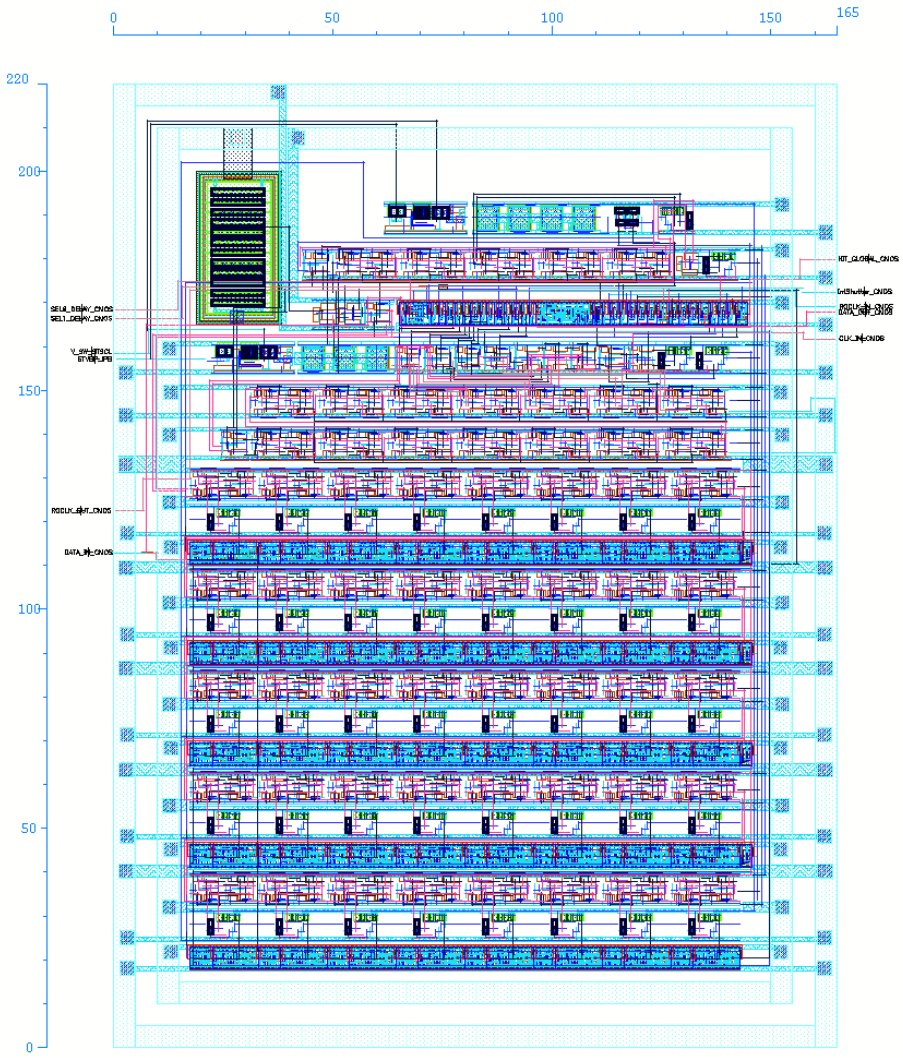


Figure 49: The layout of the final 40 bit TOA counter IP cell.

# 8 Design of a simple STSCL ADC

This section describes the design of an ADC realized with STSCL logic cells. Since an ADC is by definition a mixed signal circuit a constant current logic is very useful in this type of applications for reasons of switching noise suppression. The ADC design described in this chapter is intended to be used a front-end ASIC for the readout of detectors of ionizing radiation. The ADC will be used during ASIC calibration verifying the correct bias voltages are being applied in the analog circuit of the chip. It will be used to bin and test the ASIC dies after manufacture and it will be used during active operation of the read-out ASIC to monitor the total dark current flowing through the silicon detector sensor. The total dark current is useful for the detection of sensor faults. Measuring the dark current of the sensor will be the only measurement still providing data when the sensor is saturated, that is to say when the hit rate is so high that the charge events arriving from the sensor can not anymore distinguished from another. This state is being called pile-up. The ADC will also be used to monitor the aging (TID radiation damage) of the readout ASIC and the sensor.

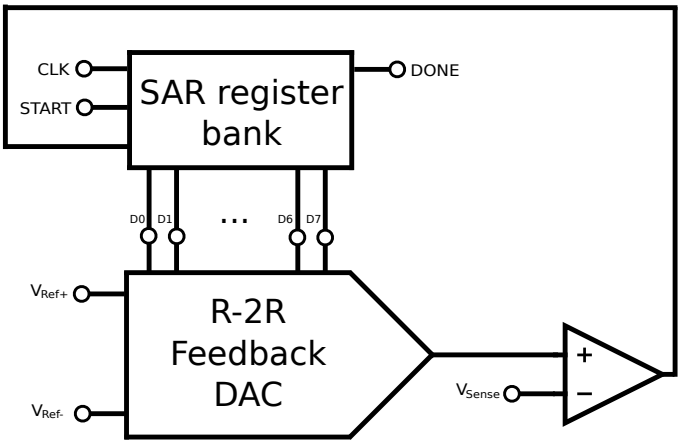


Figure 50: Simplified SAR ADC block diagram.

The ADC architecture is a simple 8-bit successive approximation ADC as is displayed on figure 50. The SAR ADC consists of three main blocks:

- The digital to analog converter which is used in the feedback loop to prepare the analog voltage for comparison. It was chosen to be realized

with a R-2R resistor based DAC for reasons of simplicity and ease of implementation.

- The discriminator was implemented with two cross-switched chopper discriminators with provide very good offset suppression and high gain. The fact that this type of discriminator needs to be clocked is not an disadvantage in this application since the ADC operation itself is too clocked.

- SAR bit bank performing the consecutive reconstruction of an unknown input signal with a halving interval search algorithm.

An attentive reader might have noticed that there is no sample and hold circuit in the ADC. The ADC is meant to measure strictly DC signals. The sample and hold circuit was omitted for reasons of simplicity. The SAR conversion process is very sensitive to noise on the sense input during the conversion process. Noise can easily cause the SAR register to make the wrong decision. It is therefore necessary to always make multiple conversions and to use a mechanism like averaging or taking the majority in case that multiple repeated conversions lead to unequal results. The ADC is neither mission critical nor does it perform time critical operations. The ADC is in its current form just a test structure and it is expected that the IP cell will undergo multiple revisions before being finalized. A sample and hold circuit will be added in one of the future revisions once the current design has been verified on silicon.

The decision to use an R-2R DAC instead of the more common charge redistribution C-2C DAC usually encountered in SAR ADCs relates to the radiation hardness of the used transistors. The transistors used in a charge redistribution DAC must withstand a gate voltage at least twice of the ADCs sensing range. That is because in the voltage at the input stage of the discriminator can rise to VREF plus the sensed input voltage. If we assume rail to rail operation the worst case input voltage can thus be twice the supply voltage. Since we wish to maintain a possible input voltage range from 0 V to 1.8 V, but cannot use for reasons of radiation hardness 3.3 V transistors, the use of a charge redistribution DAC was abandoned. The price of having R-2R DAC in the feedback loop is a larger RC settling constant between the SAR sense operations and also a higher power consumption and thus a lower figure of merit than is currently achievable with architectures utilizing charge redistribution DACs. The current design is not yet final and it is expected

that in the future a solution with a C-2C DAC can be found, which will be implemented in the next version. It will be necessary to reset the C-2C DAC after each SAR sense operation. The issue is complicated by the fact that the chopper discriminator acts as a charge pump and affects the charge stored in the C-2C DAC.

## 8.1 Discriminator design

The simplest discriminator is a differential amplifier followed with amplification stages to push the amplified signal difference into saturation (output either VDD or GND). Other possible circuits are decision circuits, which are basically bistable toggle circuits operating on the principle of positive feedback. Such circuits are usually not able to operate rail-to-rail, which is one of the requirements for the ADC. Another requirement is low offset voltage.

The choice to use a chopper discriminator is based on its superior property of having very low offset voltage and high gain in the whole ADC input range. The chopper discriminator is AC coupled and thus enables rail to rail operation. The necessity to clock the chopper does not represent a significant overhead, since the SAR ADC is clocked anyways. Its biggest disadvantage is that while it performs measurements charge is transferred to and from the input pins of the chopper. It behaves defacto like a charge pump when performing a measurement. That charge transfer is, albeit being deterministic, depended upon unknown variables (the measured voltage) and therefore the DAC outputs must have a reasonably low output impedance for the circuit to function properly. This is makes the use of a C-2C DAC in conjunction with a chopper problematic.

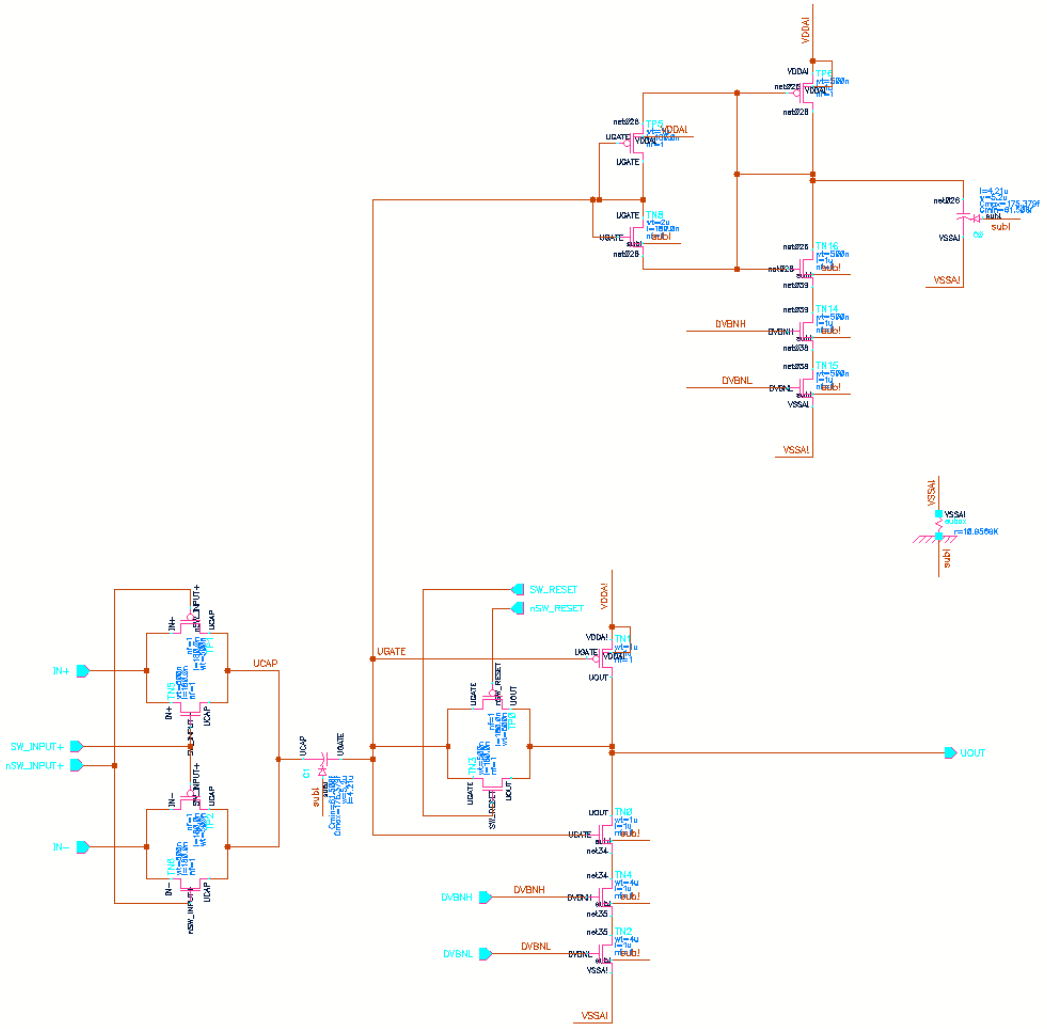


Figure 51: The schematic of the chopper discriminator. To the left is the input analog multiplexer, which switches between the reference voltage and the sense voltage. In the middle is the coupling capacitor and the reset switch. To the bottom right is the inverting push-pull amplifier stage. On the upper right is the clamp diode circuit preventing the induced voltage to exceed 500 mV to either side of the working point.

The chopper circuit operates in four phases:

- Phase 1: The chopper is reset, that is the switch connecting its output to its input is enabled and the circuit moves to the point of maximum gain.
- Phase 2: The chopper is connected to the reference voltage. Charge is moving through the AC coupling capacitor, but since the chopper is in reset the charge has no effect and is neutralized.
- Phase 3: The reset switch is now closed disconnecting the input of the inverter from its output. The input of the inverter amplifying stage is now floating and initialized at its point of highest gain.
- Phase 4: Since the AC coupling capacitance is much larger than the input capacitance of the amplifying inverter stage any change of voltage on the AC coupling capacitance will now feed through to the inverter input. Now the analog multiplexer on the input of the chopper is toggling from from the reference voltage to the sensed voltage. Any difference between the sensed voltage and the reference voltage will be amplified by the inverter stage.

The disadvantage of the chopper discriminator is that when operating it acts like a switched capacitor resistor connected between the input rails. The effective resistance between the inputs is given in equation 25.

$$R_{\Delta in} = \frac{\Delta U_{in}}{I_{in}} = \frac{\Delta U_{in}}{2 \cdot C_{in} \cdot \Delta U_{in} \cdot f_{sw}} = \frac{1}{2 \cdot C_{in} \cdot f_{sw}} \tag{25}$$

For the designed discriminator the input capacitance $C_{in}$ is non-linear since many of main contributing elements are formed by MOSFET gate capacitances. By simulation is was determined to be maximally 20 fF, thus the effective input resistance for a clock signal of 1 MHz is 25 MΩ. Another disadvantage of the chopper circuit is that it has a minimum clock speed at which it may operate. It cannot remain in phase 3 or phase 4 too long since leakage currents entering/exiting the floating input node will gradually affect the behavior.

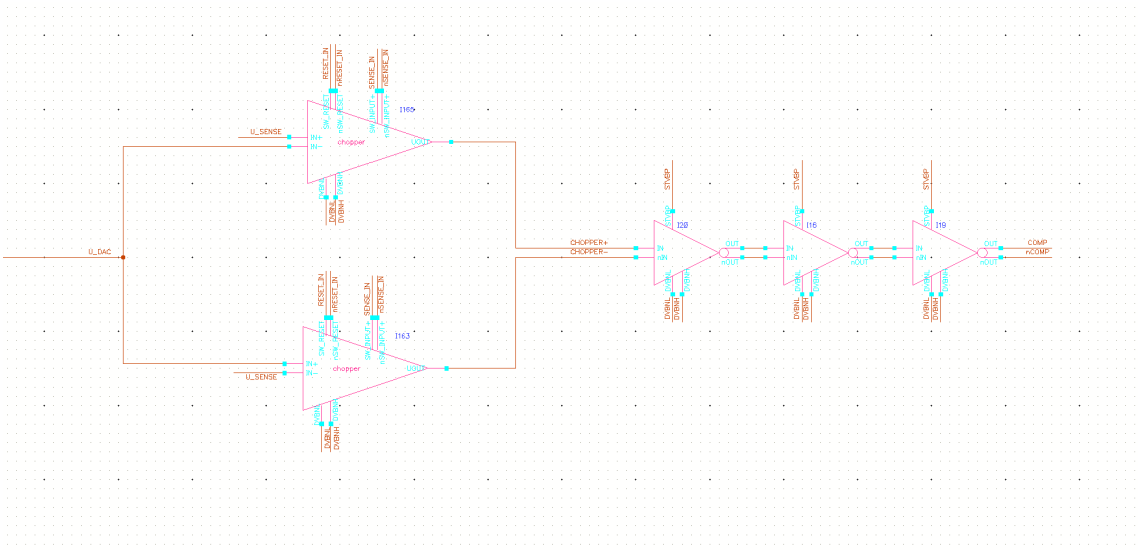


Figure 52: The schematic of the final discriminator circuit with the two counter-phase choppers and a three follow-up STSCL gain stages.

As can be seen on figure 52 the actual discriminator consists of two choppers connected in counter-phase. Counter-intuitively this does not help to neutralize the switching charge injection, because the choppers are always transporting charge from the higher input voltage to the lower input voltage. The reason to use two choppers in counter-phase is that it provides double the amplification and the following STSCL amplifying inverter stages do need a differential signal anyways. Due to mismatch variations in the two chopper circuits the reset output voltage will not be perfectly identical. There will be an offset between the output voltages of the two choppers if both in the reset state. It is though to be noted that this mismatch happens after amplification, whereas with differential amplifiers the mismatch occurs before amplification. If we project that offset back to the input of the choppers it has to be divided by the gain of the amplification stage of the chopper. The two sigma (95%) worst case output offset voltage has been measured to be 19.2 mV, but the lowest observed gain is 120, this means that the effective input offset voltage is only 160 $\mu$V which is a very low value considering how small, simple and low power this circuit is.

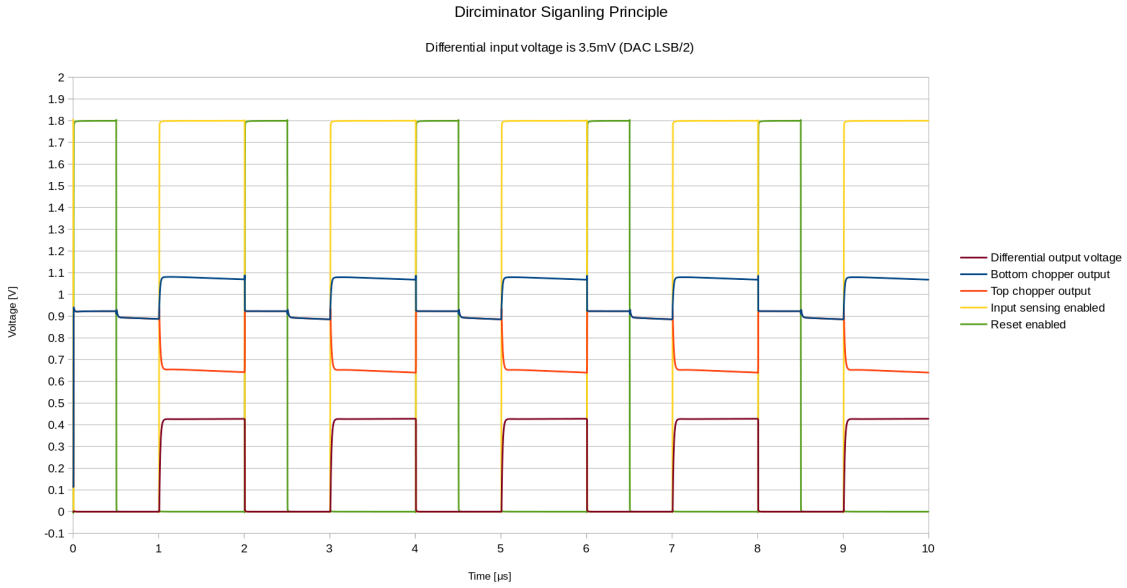


Figure 53: A transient simulation of the discriminator circuit displaying the four operating phases. The difference on the input is 3.5 mV or half a LSB of the ADC.

Figure 54 displays a transient Monte Carlo simulation of the discriminator operation. Figure 55 displays the same transient Monte Carlo simulation as on figure 54, but this time with the internal circuit noise added. As can be seen the simulation predicts, that the discriminator should not fail to reliably discriminate a LSB/2 ADC input signal difference. Simulation on the subject of common mode rejection and power supply rejection were also undertaken. The common mode rejection ratio (CMRR) is excellent, defacto not measurable, due to the capacitive coupling of the decision circuit to the input terminals.

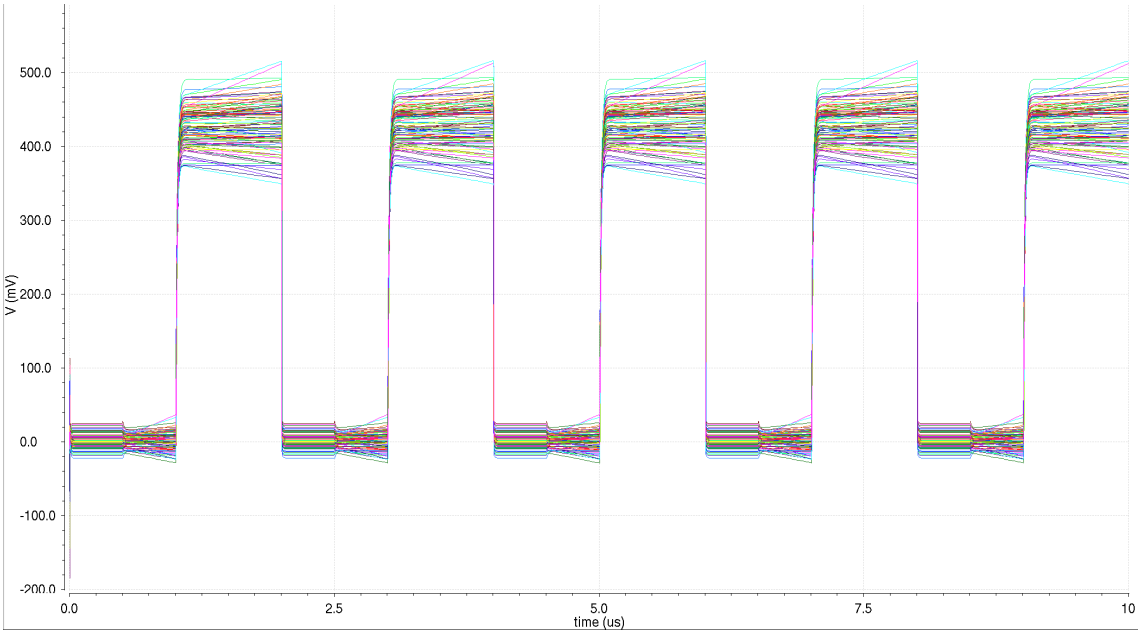


Figure 54: A transient Monte Carlo simulation of the discriminator. The displayed voltage is the differential voltage on the output. Sense frequency 500 kHz, discriminated input voltage 3.5mV. Process and mismatch variations included.

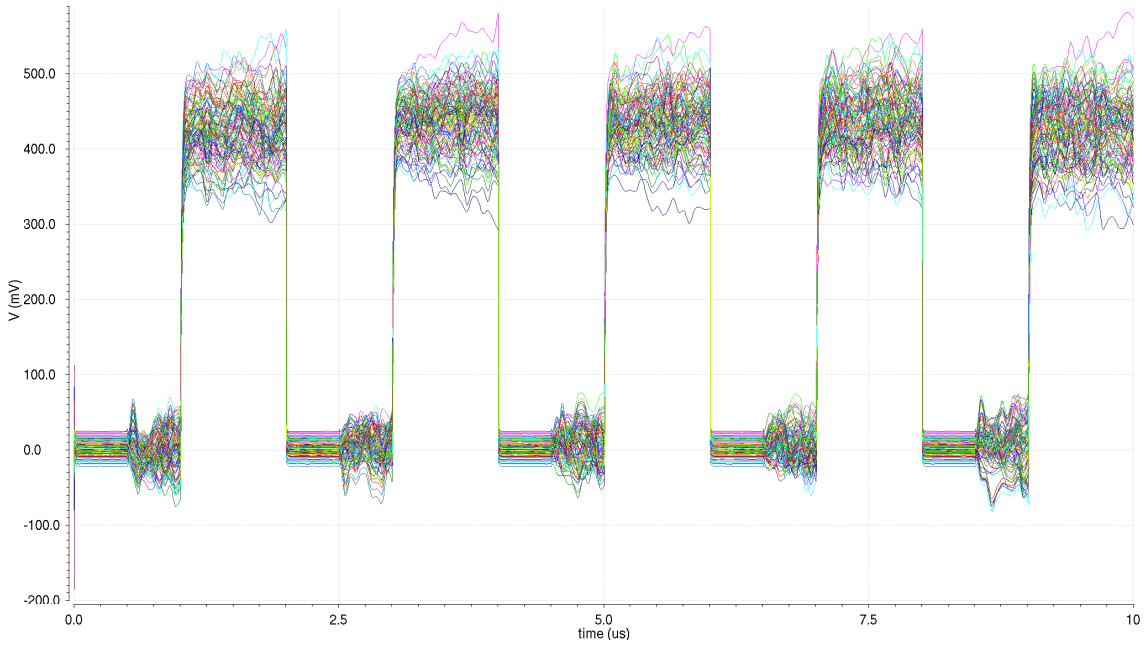


Figure 55: A transient Monte Carlo simulation of the discriminator with noise. The displayed voltage is the differential voltage on the output. Sense frequency 500 kHz, discriminated input voltage 3.5mV. Process and mismatch variations included.

The layout of the chopper can be seen on figure 56, the final IP cell has a layout dimension of 22 $\mu$m $\times$ 18.6 $\mu$m.

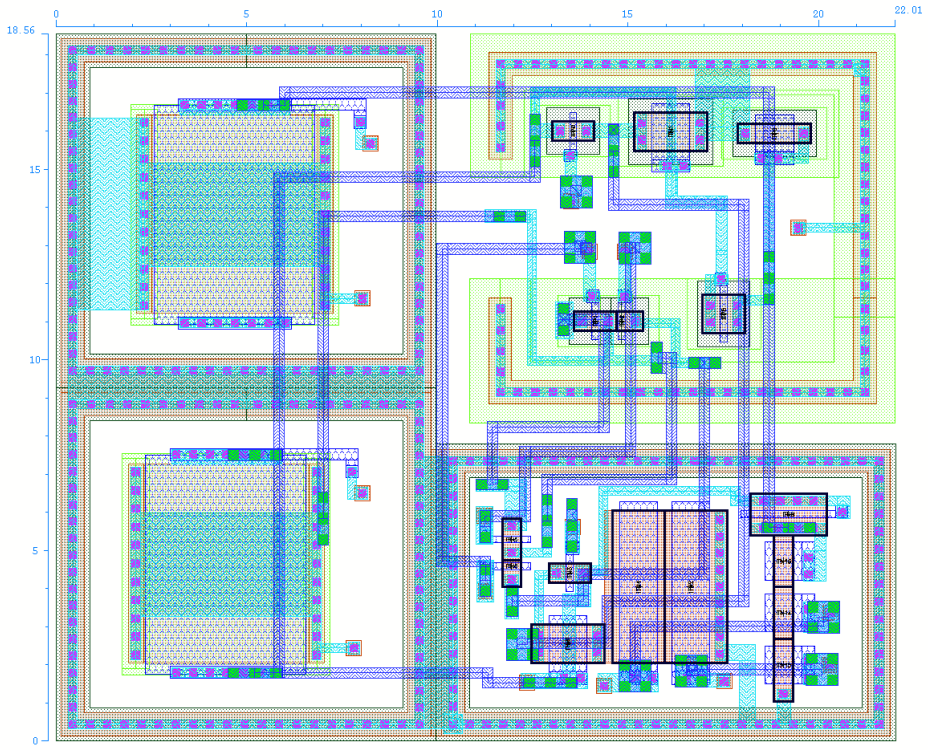


Figure 56: The layout of the final chopper discriminator circuit.

Table 2 summarizes the properties of the designed chopper circuit.

| Parameter | Value |
|---|---|
| Input offset | 160 $\mu$V |
| Max small signal gain (chopper) | 120 |
| Max small signal gain | 16 000 |
| Bias current (per chopper) | 1.125 $\mu$A |
| Static analog power | 4 $\mu$W |
| Static digital power | $12 \times I_{Tail} \times V_{Supply}$ |
| Effective input resistance | $25T\Omega \times \tau_{Switching}$ |
| Input ranges | rail-to-rail |
| CMRR | $>$ 100 dB |
| Area of IP cell | $410m^2$ |

Table 2: The parameters of the designed discriminator.

## 8.2 STSCL SAR register

The SAR register is a small digital block. The ADC has as many SAR registers as it has nominal bits of resolution. Each SAR register implements the function of the finite state machine depicted on figure 57.

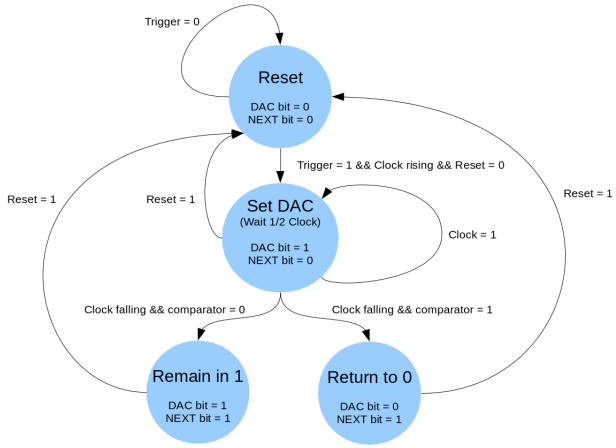


Figure 57: The state diagram of the successive approximation bit register.

Each SAR register controls a single bit of the feedback ADC. Initially the bit is zeroed. Once the SAR register is triggered it tests (sets) the DAC

bit and performs with help of the discriminator a check whether the DAC output voltage is now higher or lower than the input voltage. Depending upon if the sensed analog input voltage was higher or lower then the new DAC output voltage the SAR register decides whether to keep the DAC bit set or if it should reset the DAC bit. Once the SAR register is done testing its corresponding DAC bit it will signal the next SAR register in the ADC SAR register bank to execute the same finite state machine. The next SAR register will operate on a lesser significant DAC bit. The whole SAR conversion process executes a halving interval search algorithm trying to determine an input code word to the feedback DAC such that the DAC output voltage will equal the input voltage to be measured with the ADC. The SAR conversion process always starts at the most significant DAC bit and finishes on the least significant bit of the feedback DAC. Once all SAR registers have been triggered the ADC conversion is finished and the SAR registers now contain the digital codeword representing the analog input voltage.

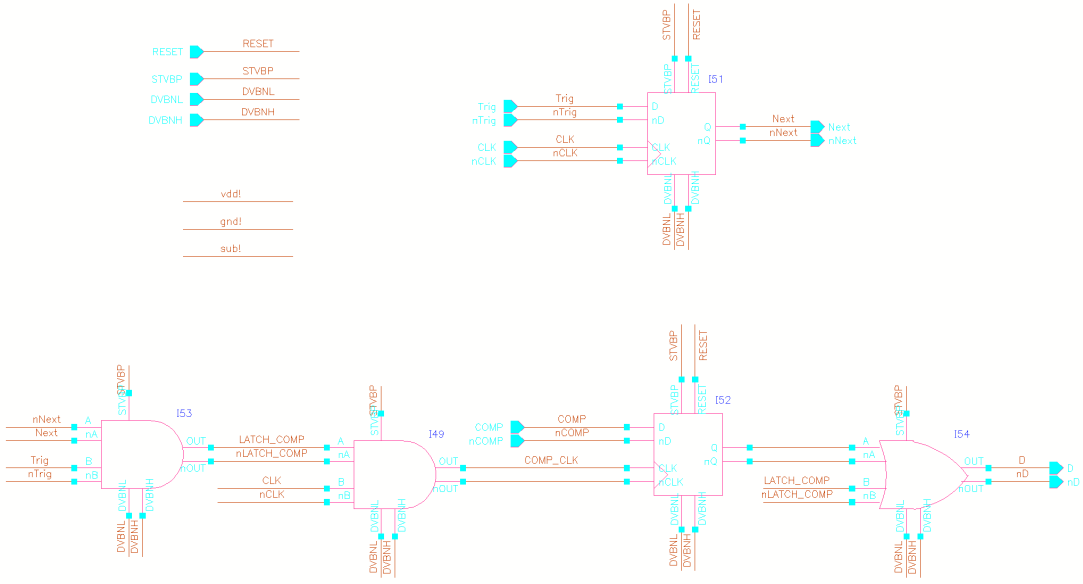


Figure 58: The schematic of the STSCL successive approximation bit register.

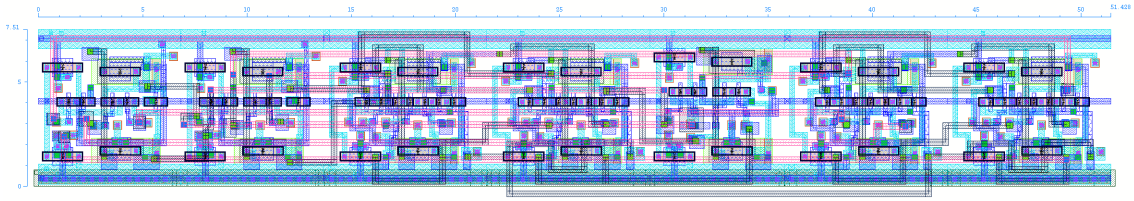

Figure 59: The layout of the STSCL successive approximation bit register.

## 8.3 Feedback DAC design

Another important sub-circuit of the ADC is the feedback digital to analog converter (DAC). It is used to generate a voltage signal, that is being compared with the unknown input voltage to be measured. The feedback DAC must be highly linear and have low INL and DNL, since any such error would become part of the transfer function of the ADC. There are multiple possible DAC architectures possible to be used as feedback DACs. The most typical is the charge sharing DAC, which is a circuit structure consisting of capacitors of various sizes (usually powers of 2). By switching a known voltage into one terminal of the a capacitor a known charge is being transfered across the capacitor. By summing the charges on a common capacitor connected to a virtual ground the output voltage of the charge sharing DAC is generated. Charge sharing DACs are preferred in SAR ADCs due to their excellent power efficiency, reasonable linearity (Capacitors are circuit elements with a high process error, but low mismatch error. Since the output voltage is not a function of the absolute value of the capacitance, but only of the relative size of the capacitances such structures display very low PVT variance.) and their switched nature is not a drawback in this application since the SAR DAC is itself a switched circuit. However is was decided not to use a charge sharing DAC in this application. The reason is twofold. The first reason has to do with radiation hardness. The ADC shall be rail to rail and at the same time radiation hard and therefore can utilize only 1.8 V transistors. A charge sharing DAC can under certain conditions generate voltages in excess of twice its input output range, which would imply that 3.6 V transistor would be needed in the discriminator input stage. Another reason against the C-2C DAC is that the chopper discriminator has a finite input impedance and a

voltage buffer between the DAC and the discriminator would be needed for impedance matching. This added buffer would add nonlinearity and complexity. A R-2R DAC is a very simple, very robust, extremely radiation hard DAC which has reasonable linearity in 8 bit resolution. The R-2R DAC has, for the same reasons as the C-2C DAC, a very low PVT sensitivity. The output voltage of the DAC does not depend upon the absolute value of the resistors used, it only depends upon the relative resistance. In CMOS processes resistors are circuit elements which display a high process variation (the resistance can be $\pm 30\%$), but the mismatch variation is very low (the resistors can be easily matched with $\pm 0.2\%$ precision). A disadvantage of the R-2R DAC is that it has a static power consumption and is slower than a charge sharing DAC. Figure 60 displays the schematic of the R-2R feedback DAC used in the ADC. The DAC has a very simple structure.

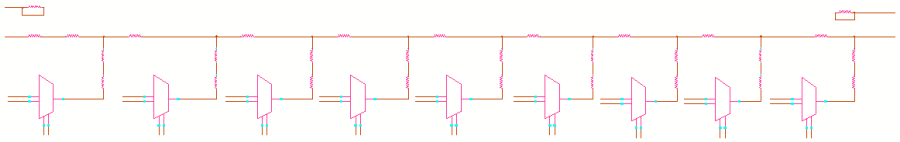

Figure 60: Schema of the feedback DAC.

Figures 61 and 62 display the INL and DNL Monte Carlo simulations of the designed DAC. The LSB of the 8 bit ADC at a supply voltage of 1.8 V is 7 mV. As can be seen not a single INL Monte Carlo case is exceeding in the worst case one LSB which means the designed DAC is suitable to be used in an 8 bit SAR ADC.

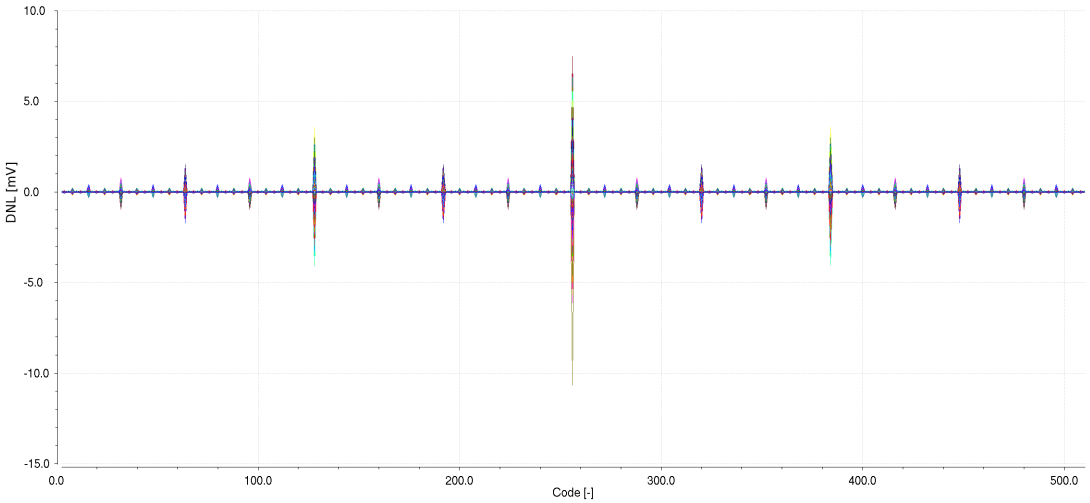


Figure 61: Feedback DAC DNL Monte Carlo simulation.

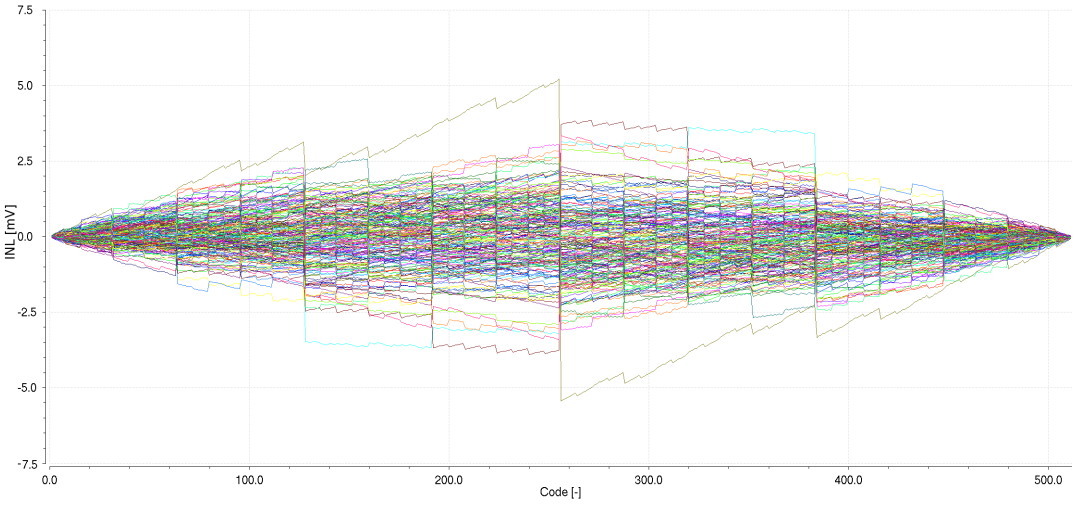


Figure 62: Feedback DAC INL Monte Carlo simulation.

Figures 63 and 64 display the statistical distribution of the worst case DNL and INL of the designed R-2R DAC extracted from the Monte Carlo simulations. The mean worst case DNL is 400$\mu$V with a standard deviation of 2.51 mV and the mean worst case INL is 238$\mu$V with a standard deviation of 1.27 mV.

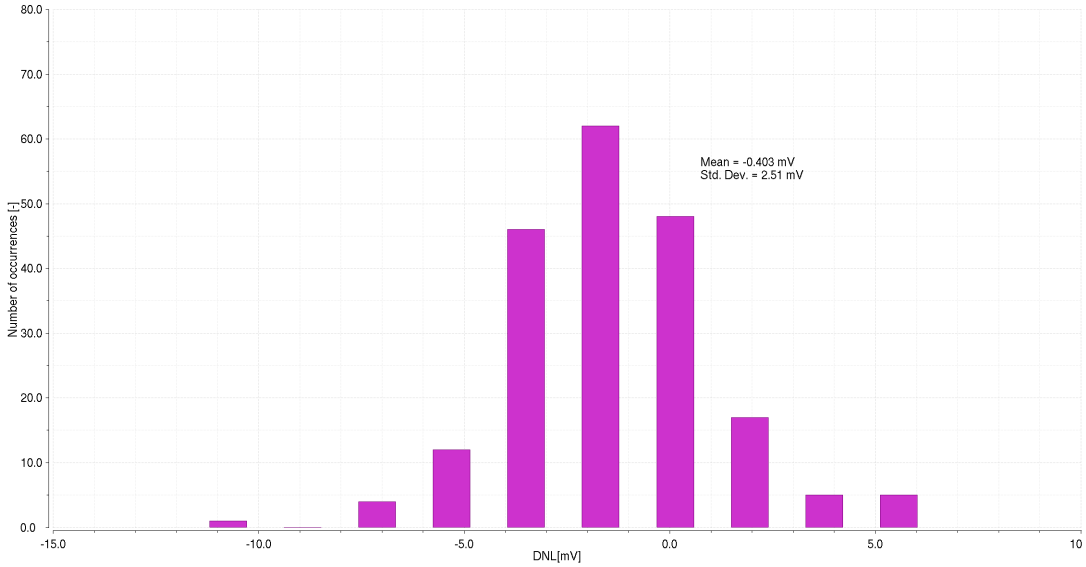


Figure 63: Feedback DAC worst case DNL distribution Monte Carlo simulation.

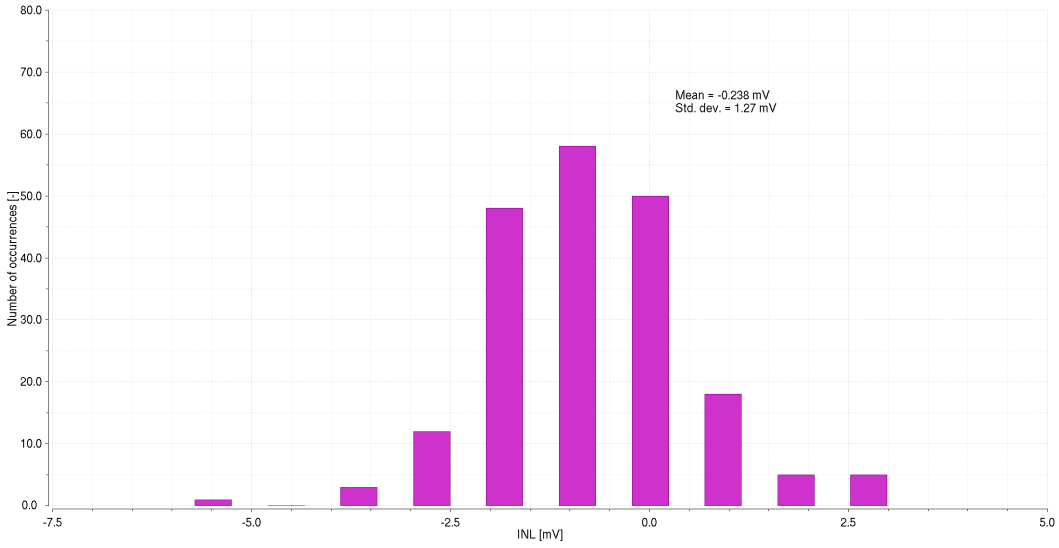


Figure 64: Feedback DAC worst case INL distribution Monte Carlo simulation.

## 8.4 The final ADC design

With the IP blocks described in the previous subsection the final ADC was assembled. The schematic of the final ADC can be seen on figure 65. Even though the ADC is to be used as a 8-bit ADC it has been designed with 9 nominal bits. The additional bit will be used for testing and to verify the ADC design.

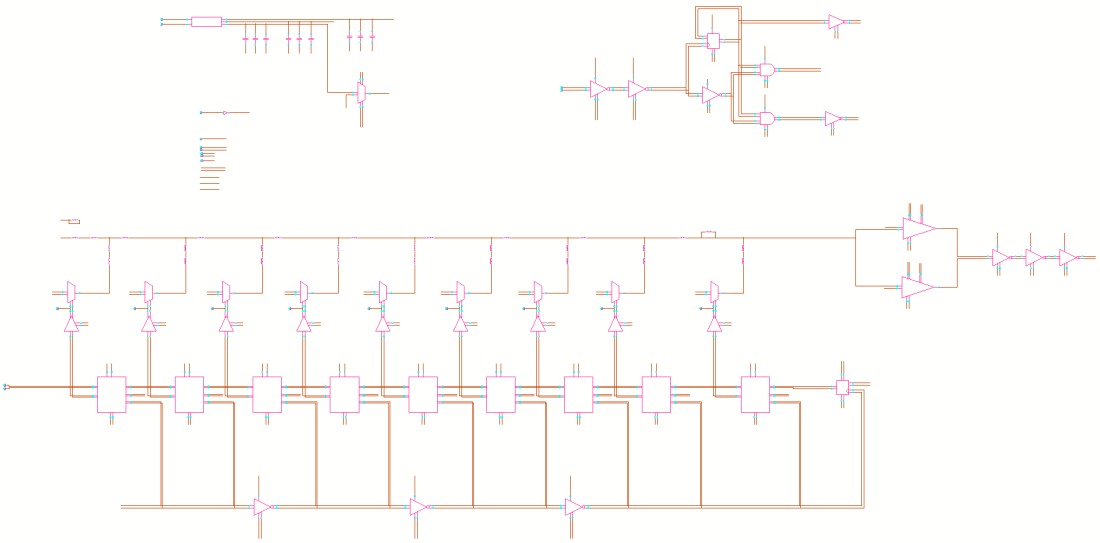

Figure 65: The schematic of the constant current SAR ADC. Upper left is the biasing network. Upper right is the clock conditioning network. To the left are the two chopper discriminators. In the center is the R-2R feedback DAC driven by the SAR register bank.

In order to synchronize the individual IP cells a clock conditioning circuit has been designed. The schematic of the clock conditioning circuit can be seen on figure 66. The clock conditioning circuit makes sure that the SAR registers and the discriminator receive the correctly timed clock edges and operate smoothly together.

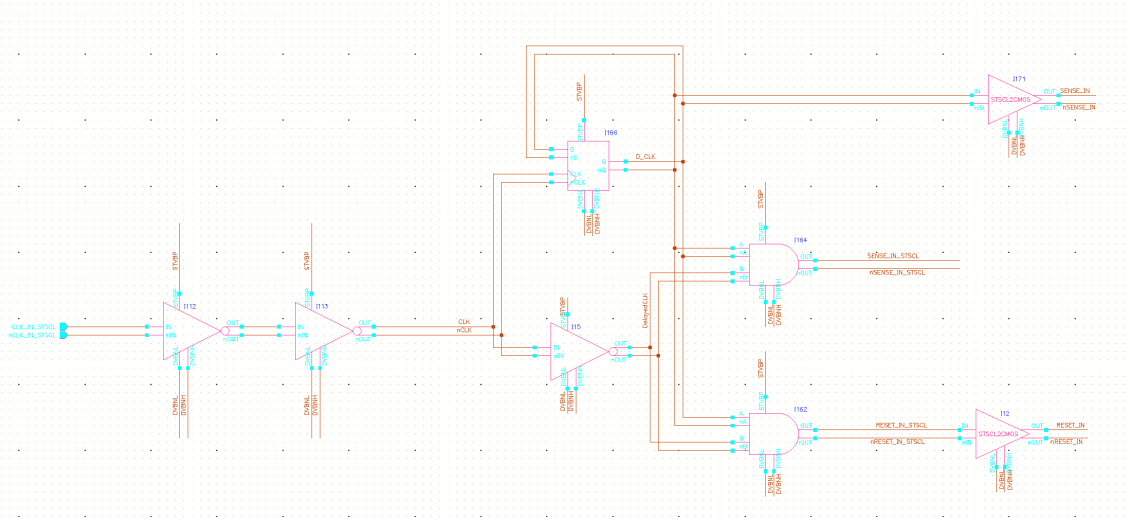

Figure 66: The ADC clock conditioning circuit.

Figures 67 and 68 display a transient simulation of the ADC performing an conversion. The ADC has constant current consumption of 245$\mu$A with a ripple current of roughly 30$\mu$A. The ripple current is caused by the analog switches toggling in the discriminator and the switching of the DAC not the digital logic.

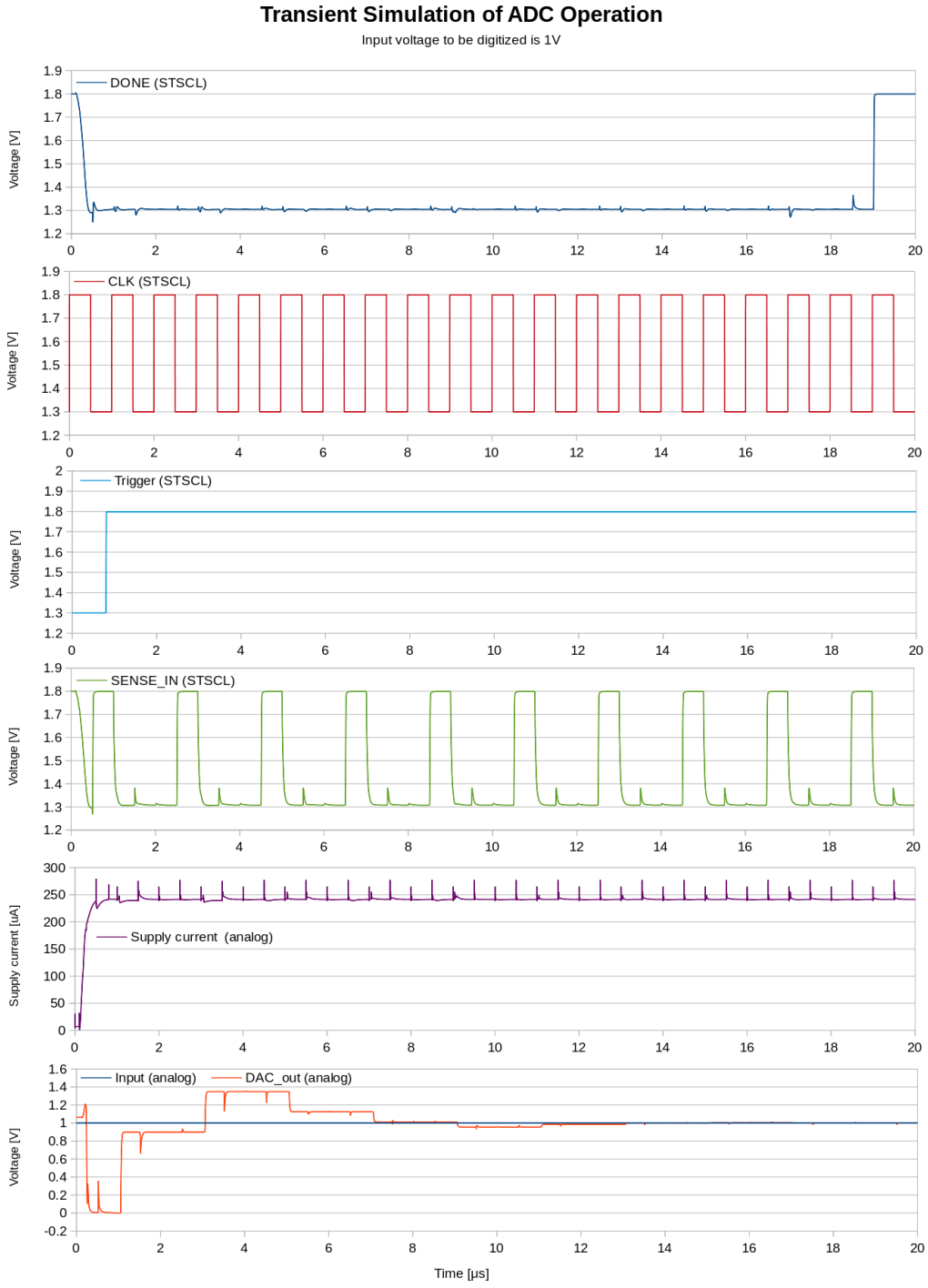


Figure 67: Transient simulation of ADC operation.

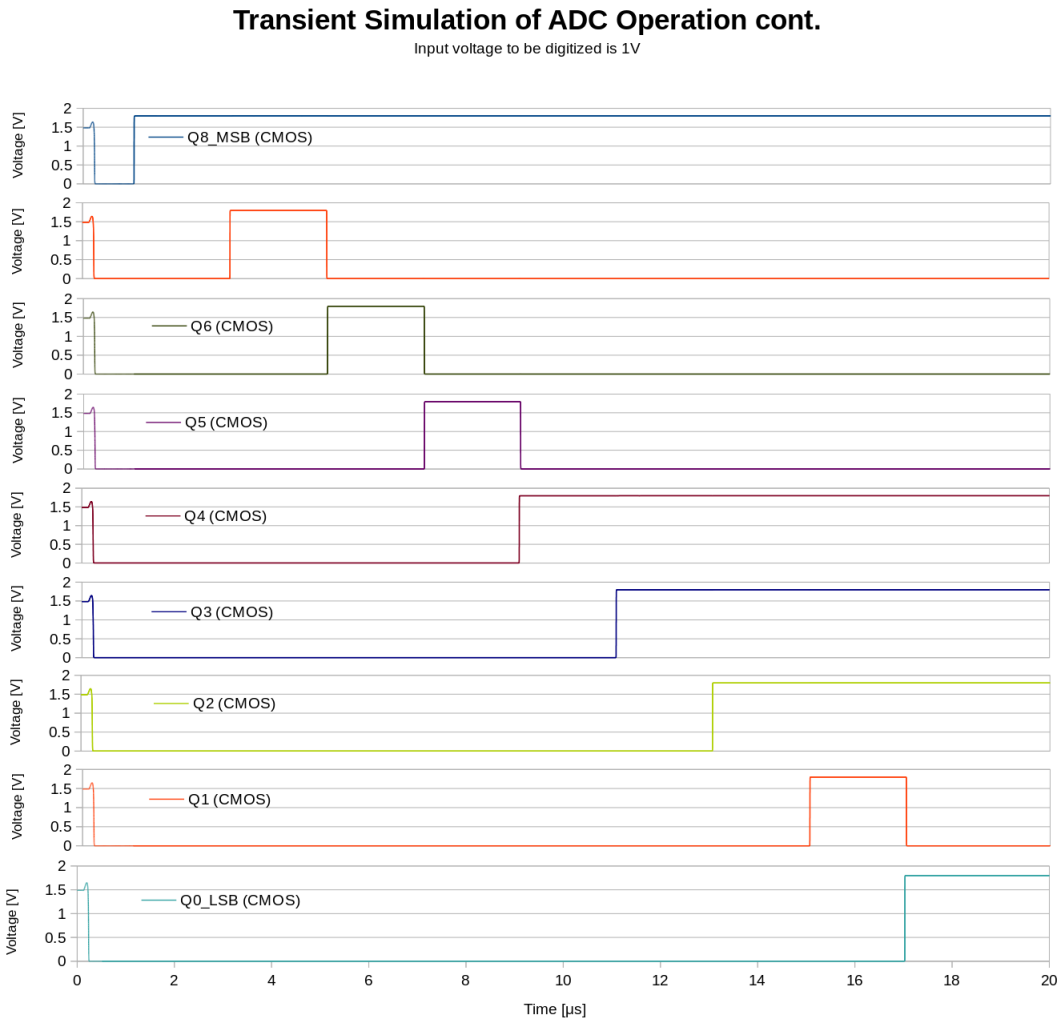


Figure 68: Transient simulation of ADC operation continued.

Figure 69 displays the final ADC layout together with a digital CMOS wrapper circuit to enable access to the ADC from the outside CMOS domain. The CMOS logic is not active when the ADC is operating. The final ADC IP cell has a size of 184 $\times$ 167 $\mu$m.

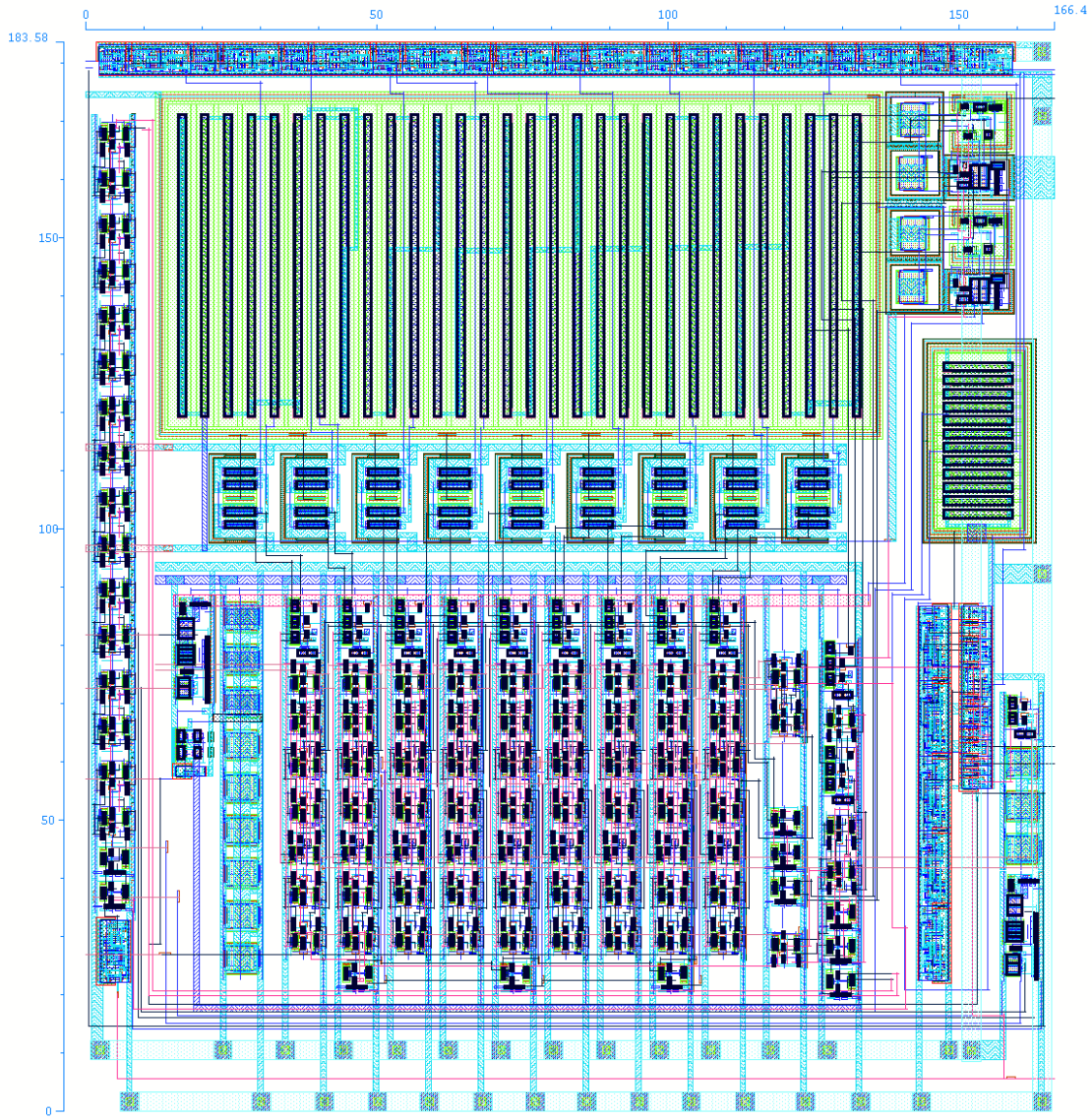


Figure 69: The layout of the final constant current SAR ADC together with the digital CMOS wrapper.

# 9 Conclusions

A standard cell library of STSCL gates was developed for the use in low gate count digital IP cells in front end nuclear detector ASICs. Nuclear detector readout requires ultra low noise circuitry. The removal of simultaneous switching noise caused by digital circuits is the most sought after feature of the STSCL implementation covered in this thesis. The fact that STSCL is usually meant to be designed for ultra low power applications was only a secondary design concern and the library has not been designed for very low supply voltage operation. The key design goal was it to have mixed signal measurement circuits which display a constant current consumption during operation. The cells are to be used in the analog design flow and only one drive strength has been implemented for each type of logic gate. By simulation it was determined that the test circuits can be operated with a minimum supply voltage of around 1 V. This limitation for the minimum supply voltage stems from the analog amplifiers used in the biasing feedback networks. It is not expected that the cells will ever be operated with a different supply voltage than the process voltage of 1.8 V.

The implemented standard cell library contains the basic logic gates such as a buffer/inverter, and/nand, or/nor, xor/xnor, D-latch and a master slave D-flip flop. The tail current and the switching voltage swing can be set by an internal 8 bit voltage DAC or an external high precision voltage source. With the internal DAC the tail current can be set from 30 nA up to 7 $\mu$A. The tail current is physically limited with a transconductor circuit to prevent accidental opening the parasitic PNP transistor in the load PMOS devices and the creation of dangerous latch-up conditions. The maximum logic level voltage swing is 500 mV. In the slowest simulation corner the maximum operation frequency 200 MHz for the highest tail current setting and can be as low as 1 KHz for a tail current close to the leakage currents. The static noise margin was determined to be $NM_{STSCL} = 230mV$ at a voltage swing of 400 mV. The necessary support circuits were also designed and tapped out. The support circuits contain the bias voltage circuit used generate the two tail current reference voltages and the reference voltage to set the resistance of the load PMOS devices. Additional implemented support circuits are the STSCL to CMOS level shifters. The designed cells fit into a grid with a vertical pitch of 7.42 $\mu$m. The layout of the cells enables easy butting in arbitrary order without causing any DRC errors. The tail current bias rails and the switching voltage swing bias rail are automatically connected if cells

are placed next to each other.

As simple time of arrival counter to be used in a nuclear detector ASIC was implemented with the function of a delayed shutter. The static current consumption of the counter is 205 times the set tail current. The size of the TOA counter cell is 165 $\times$ 220 $\mu$m.

As an additional test structure a complete 8-bit SAR ADC was designed. The ADC uses a resistive R-2R ladder as the feedback DAC and a switched discriminator with offset suppression. The ADC has a rail-to-rail operation range. The current consumption of the ADC is 5$\mu$A plus 243 times the tail current. The size of the ADC cell is 184 $\times$ 167 $\mu$m. From the outside world the ADC and TOA counter IP cells are accessible through shift registers with CMOS signals. The ADC can be used only to sense DC signals since it has no sample and hold circuit.

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